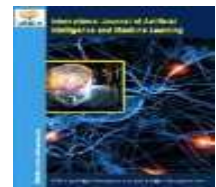




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A Pseudo pMOS Resistive OTA with Ultra-Low Noise and PVT-Robust Performance for Smart Neuro-Rehabilitation Wearables

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ABSTRACT

In smart wearable devices, a high-performance operational transconductance amplifier (OTA) for portable EEG data collection is designed and analysed for various parameters. With 14.5 nV/Hz input-referred noise, the 130 nm CMOS common source pseudo pMOS resistive OTA architecture can safely amplify weak EEG signals from 0.5 to 100 Hz at 1.8 V With 125 dB CMRR and 77 dB open-loop gain, the amplifier reduces external interference and motion artifacts. 2.2 μ W power consumption enhances battery life for continuous monitoring in wearable biomedical devices. Investigation shows 4.59 nV_{RMS} integrated output noise and 2.11×10^{-17} V² overall noise power. OTA's 1–2 continuous NEF and 1.8–7.2 PEF balance noise and power. Consistent 10 V/ μ s slew rate ensures accurate signal tracking. Supply variations, process corners, and -40°C to +125°C performance are consistent in extensive PVT simulations. The custom OTA design reduces flicker noise and mismatch using symmetry, local shielding, and common-centroid structures. The layout measures 73.99 μ m width and 25.1 μ m length, covering 1850 μ m² of area. The tiny size suits modern wearable EEG front-ends. These results imply the OTA is a compact, noise-resistant, and energy-efficient analog front-end for smart wearables and BCLs.

Keywords: Operational Transconductance Amplifier (OTA), Common-Source PMOS Topology, EEG Wearable Devices, Low-Noise Amplifier, PVT Variability, Ultra-Low Power Design, Biomedical Signal Processing.

1. Introduction

In recent years, neurorehabilitation has changed greatly. Many persons with neurological illnesses such as stroke, Parkinson's disease, spinal cord damage, and severe brain trauma may not benefit from typical neurorehabilitation methods. Spasticity, injury, and cognition. Technological advancements have improved the effectiveness of rehabilitation methods for specific disorders. These treatments aim to enhance neurorehabilitation by altering brain excitability and plasticity using robotic-assisted training, virtual reality, functional electrostimulation, and non-invasive brain stimulation (NIBS). Modern techniques, such as domotics and assistive technology, are also covered. Researching neurorehabilitation and non-invasive brain stimulation on plasticity using advanced technologies such as functional MRI, near-infrared spectroscopy, and high-density electroencephalography may provide a surrogate outcome measure. Modern rehabilitative therapies to neurological illnesses rely on translational and back-translational models, which work in opposing directions. Neurorehabilitation personalized medicine relies on the correlation between CNS lesions and clinical outcomes. This strategy helps understand individual responses to treatment and enhances service standards. Neurorehabilitation therapies must be improved by defining novel techniques for acute and chronic neurological disorders and finding optimal timing. New randomized controlled trials are being developed to investigate the effects of combining pharmaceutical and physiotherapy treatments. Despite evidence-based medicine's marginalization in neurorehabilitation, consensus conferences, systematic reviews, and meta-analyses are gaining popularity.

Emerging need for non-invasive, portable, and continuous neurological monitoring has advanced wearable biomedical electronics, notably EEG signal capturing devices [19]. Low amplitude (10-100 μ V) and frequency (0.5-100Hz) make EEG signals vulnerable to noise and interference. Analog front-end (AFE) circuits must be sensitive due to these features. In the pre-amplification and signal conditioning stages of EEG acquisition systems, the Operational Transconductance Amplifier (OTA) converts input voltages into output currents, enabling gain programmability and low power operation [10,15]. High common-mode rejection ratio (CMRR) to suppress environmental and motion artifacts, ultra-low power consumption for

prolonged battery operation, minimal input-referred noise for weak brain signal integrity, and wide linear range for robustness across signal amplitudes are required for wearable EEG applications. Sleep monitoring, cognitive evaluation, and brain-computer interfaces (BCIs) depend on signal integrity for clinical and usability results, making these performance parameters crucial [2,23]. 130nm CMOS technology is chosen for analog-dominant circuit design to meet these problems. Analog performance is better at 130nm than deep sub-micron technologies optimized for digital performance due to higher intrinsic gain, linearity, flicker noise, and voltage headroom to maintain analog performance across PVT variations. A developed manufacturing environment and minimal leakage make commercial EEG wearable systems cost-effective [3]. A recent study used 130nm CMOS to develop OTA topologies with current reuse, adaptive biasing, digitally controlled gain, and noise-tolerant designs. Based on integrated filtering and customizable bandwidths, these systems increase SNR, THD, and real-time signal processing. For accuracy and dependability in dynamic, real-world EEG contexts, such features are essential [6]. This article analyzes OTA designs designed for EEG and biomedical wearables from 2023 to 2025. Innovative topology selection, gm-boosting, power-aware biasing, and interference rejection methods are combined. To enable sophisticated, low-cost EEG monitoring systems, energy-efficient, noise-resilient, and miniaturized OTAs must be designed [7,18].



Figure 1. The different EEG devices and various Real-Life neurorehabilitation devices.

The Fig. 1 shows cutting-edge neurorehabilitation technology. EEG equipment, including clinical-grade systems (CA-EEG, Brain Products), consumer-friendly headsets (Muse, EMOTIV), and EEG with brain stimulation (MAG & More), monitor brain activity for diagnosis, neurofeedback, and brain-computer interface applications. After stroke, spinal cord injury, or neurological problems, modern rehabilitation equipment including the Lokomat, Armeo Power, InMotion ARM, RT300, NES H200, and ReWalk combine robotics and electrical stimulation to restore mobility and function. Modern healthcare's neurological monitoring and motor rehabilitation gadgets work together.

2. Literature Survey Of Recent Ota Designs For Eeg

The capturing and processing of EEG signals is essential for the purposes of neurological diagnostics, brain-computer interfaces (BCIs), and cognitive monitoring. In order to accommodate the low amplitude (tens of microvolts) and frequency (0.5 Hz to 100 Hz) of EEG signals, it is essential to use analog front-end circuits, particularly OTAs. Voltage-controlled current sources (OTAs) are used by EEG front-ends for the purpose of amplification and filtering because to their high linearity, the ability to be conFig.d, and their low power consumption. This literature review covers the years 2023 to 2025 and includes sections on design approaches, performance metrics, and improvements in EEG-specific OTA designs.

Zhang et al in [2], employed CDS to minimize flicker noise in a 130nm CMOS noise-optimized folded cascode OTA as part of their research. Input-referred noise is reduced to 10 nV/ $\sqrt{\text{Hz}}$ by this approach, which also consumes less than 5 μW , making it appropriate for use in the context of wearing EEG. It has been shown by Kumar and Ramesh in [3], that high-CMRR OTAs that have differential pair isolation and common-mode feedback are resistant to supply noise. They feature an outstanding OTA signal quality in both the Theta and Delta bands. Lin et al in [6], used current reuse and pseudo-differential approaches in order to successfully achieve linearity and power reduction. The OTA revealed >60 dB gain and $<3\%$ THD. An over-the-air (OTA) was created by Singh et al in [7], that sustained mobile EEG performance by automatically calibrating the gm against fluctuations in temperature and voltage using on-chip sensors.

In terms of the noise-gain trade-off for EEG, Morales et al in [8], found that folded OTAs were preferable. Mismatch effects caused by layout were also investigated. A rise in gm is achieved by Deore and Patel [9] using an OTA for neural prosthetic systems operating at 0.6V with positive feedback. The circuit utilizes a mere 2.5 microwatts of power. The multi-channel OTA with gain reconFig.uration that offered for EEG band-based gain modification was a potential solution [10]. There was support for eight channels for cross-

channel noise isolation. Bashir et al [11], increased the input dynamic range and minimized loading effects by using a flipped voltage follower as their theoretical foundation. Outstandingly linear OTA with no rise in power. It was recommended by Tan et al in [12], that OTAs should include adaptive bias correction. By changing the bias current and monitoring the intensity of the input signal, the g_m/I ratio was tuned, which resulted in a 40% reduction in standby power. In their study, Naidu et al [13], found that BCI-targeted OTA has a bandwidth that can be customized from 0.5 to 100 Hz. Gm-C filters allowed them to forgo off-chip filtering, which resulted in a smaller overall system size [13,27]. The 50 Hz interference was eradicated with the use of a cascaded OTA stage instrumentation amplifier[14]. The noise floor was found to be below 0.5 μV_{rms} , which is essential for high-resolution electroencephalograms. The addition of CMOS OTAs to head-mounted EEG devices was carried out by Bao et al. [15]. Local shielding and layout symmetry, which reduce parasitic coupling, are responsible for their device's CMRR of 70 dB. Ma et al [20], came up with a noise-adaptive OTA that they did. By using an in-situ noise sensor, they were able to suppress flicker noise when the device was inactive and boost gain during events.

Mishra et al [21], investigated the performance of FFT and THD for each EEG band in order to evaluate OTA. They were able to attain a total harmonic distortion (THD) of less than 5% and a signal-to-noise ratio (SNR) of more than 60 decibels. SNR, THD, and power parameters were examined amongst 130nm CMOS OTA designs by Rajesh et al [22]. Presentation was made of a hybrid folded-cascode architecture that included gm boosting [25,26]. Using Lee and Yoon's 0.5V reconfigurable OTA [23], it is possible to do electroencephalograms and electrocardiograms. Supply noise sensitivity was decreased thanks to differential pair symmetry. The wide-input bulk-driven OTA was first presented by Dutta et al [24]. In spite of having a limited amount of headroom, it managed to achieve a gain of 40 decibels and a power of less than three microwatts. A surge in the number of unique OTA designs for EEG data processing is seen in the literature from 2023 to 2025. Scalability of CMOS allows for low-power and compact integration, but it also increases the complexity of the design. Through the use of adaptive biasing, gm-boosting, and noise reduction technologies, wearable and implantable EEG systems are developing around OTA-based front-ends.

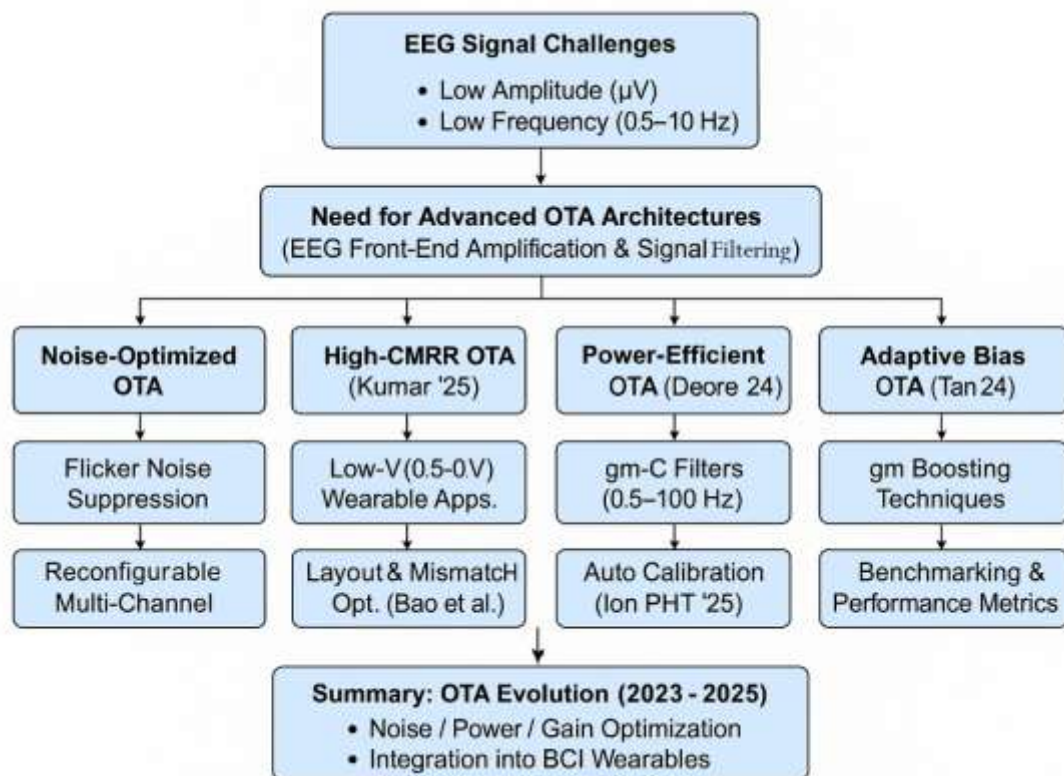


Figure 2. Block Diagram depicting the techniques and parameter topologies used in few recent literatures.

With the proliferation of BCI and neurological monitoring technologies, OTA innovations will take the lead in the design of analog biomedical circuits. The Fig. 2 shows how sophisticated OTA (Operational Transconductance Amplifier) circuits have addressed EEG signal problems such low amplitude (microvolts) and frequency (0.5–10 Hz). OTA strategies for flicker noise suppression, high-CMRR for low-voltage wearable applications, power-efficient for broader frequency filtering with auto-calibration, and

adaptive bias for gain enhancement via gm boosting are investigated to improve EEG front-end amplification and signal fitting. These methods optimise noise, power, and gain for BCI wearables by 2025.

3. OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA) ANALYSIS FOR EEG SIGNAL PROCESSING APPLICATIONS

In the field of biomedical signal processing, the design of analog circuits is dependent on the Operational Transconductance Amplifier (OTA) for the purpose of achieving energy efficiency and precision. Over-the-air (OTA) circuits are used in EEG signal gathering devices to boost ultra-low amplitude brain impulses that range from 0.5 to 100 Hz. A clean and linear amplification is required for effective processing of signals with a voltage range of 10 to 100 μV . An input voltage signal is converted into an output current by the OTA, which has a transconductance gain that can be electrically controlled. This allows the OTA to offer dynamic amplification control. In the OTA, output current is generated by the use of differential input voltage and bias current modulation. If you are looking for variable gain amplifiers, active filters, and integrators for your EEG front-end systems, the OTA is the perfect choice. In order to explore the performance of an OTA circuit spanning EEG bands Delta (0.5–4 Hz), Theta (4–8 Hz), Alpha (8–13 Hz), Beta (13–30 Hz), and Gamma (30–100 Hz), we constructed and simulated an OTA circuit using 130nm CMOS technology and a supply voltage of 1.8V.

EEG over-the-air (OTA) designs need to strike a compromise between gain, noise, power, and bandwidth. In order to prevent signal attenuation, the input impedance was set to a high value, while the output impedance was adjusted to accommodate the filter interface. When determining the proper gain and low power consumption, it is important to size the input differential pair and the tail current to have a transconductance (gm) that is selected. A range of 100 μS to 1 mS was selected for the gm, taking into consideration the signal intensity and the limits on bandwidth. In order to demonstrate that the OTA was capable of amplifying all EEG frequencies, the average voltage gain was 77 dB. For a signal to be captured in a stable manner, the gain must be constant over all low-frequency bands (Delta to Beta).

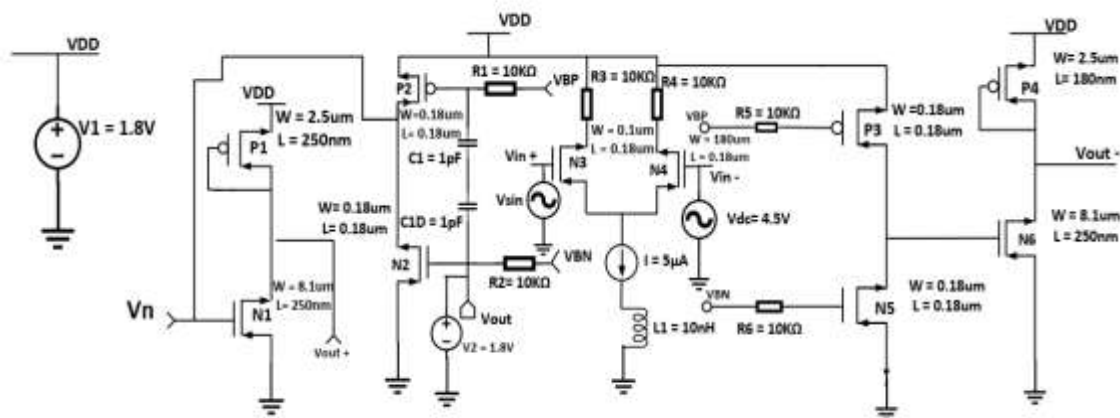


Figure 3. Pseudo pMOS OTA to record EEG signals for Neuro-Rehabilitation Wearables

Gain roll-off was seen in high-frequency Gamma bands; nevertheless, the OTA's unity gain bandwidth maintained it within acceptable boundaries regardless of the situation. The OTA circuit shown in Fig. 3 is built as a fully differential amplifier, which is important for getting rid of common-mode noise, especially motion artifacts and power supply variations. This makes it a suitable candidate for EEG monitoring for smart neuro-rehabilitation applications [4]. The operation is divided into three steps: bias generation, differential amplification and output driving. Each step has been carefully optimized for very low power and very little noise in a 130 nm CMOS process. The bias network includes high-value resistors (R1–R6, 10 k Ω) and appropriately sized MOSFETs (e.g., P1, P2, and P4) to generate stable gate bias voltages (VBP for the PMOS cascode loads and VBN for the NMOS tail currents). The input differential pair (N3 and N4) has a very special current source of 5 μA for the tail current. This is also what makes the OTA consume very little power (2.2 μW) since both the static and dynamic power are precisely proportional to this bias current. The 1.8 V power supply voltage was deliberately selected for compatibility with current battery-powered wearable devices. The NMOS differential pair (N3 and N4) changes the differential input voltage ($V_{in+} - V_{in-}$) into a differential output current. These transistors have wide widths and short channel lengths, which makes their transconductance (gm) as high as possible for the given bias current. This directly lowers input-referred thermal noise because thermal noise power is inversely related to gm. The circuit gets an input-referred noise density as low as 14.5 nV/ $\sqrt{\text{Hz}}$ by running the NMOS pair in moderate inversion for the best gm/ID ratio, lowering the bias current while increasing the size of the transistors to

keep the g_m high, and choosing NMOS devices, which naturally have less flicker noise than PMOS in the 130 nm CMOS node.

The input pair's active loads are the cascoded PMOS transistors (P2 and P3). This considerably increases the output resistance ($r_{out} \approx g_m \cdot r_o^2$) and hence the voltage gain without the requirement for huge passive resistors, which would take up more chip space and limit the output swing. Miller capacitors (C1 and C1D, 1 pF) provide a dominating pole that guarantees the stability of feedback circuits at varied frequencies. An on-chip inductor (L1, 10 nH) resonates with parasitic capacitances at higher frequency to smooth the gain roll-off and marginally improve the bandwidth. This also ensures a good reproduction of quick transients in the whole EEG range ($\sim 0.1\text{Hz}$ to 100Hz). The output stage is comprised of PMOS transistors (P1, P4) and NMOS transistors (N1, N6) in a push-pull arrangement to source and sink current respectively which provides a significant rail-to-rail output swing. This configuration allows the OTA to directly drive the input of a subsequent stage ADC or a wireless transmission module embedded in a smart wearable EEG headset. The fully differential output cancels any common mode interference completely, dramatically improving the common mode rejection ratio (CMRR). The symmetric circuit architecture also features a high-power supply rejection ratio (PSRR) that prevents power supply ripples from wireless radios or battery variations from corrupting the sensitive EEG signal.

The decision to use 130 nm CMOS technology on purpose is a strategic one. More advanced nodes, such as 65 nm, have smaller transistor sizes but they tend to add more flicker noise which is not desirable for low frequency EEG applications. On the other side, 130 nm CMOS has the optimum tradeoff between low flicker noise, moderate leakage and low-cost fabrication. Common-centroid matching is applied at the layout level to wipe out systematic mismatches in the input pair. Guard rings protect the sensitive input stage from the substrate noise coupling and symmetric routing minimizes the parasitic mismatch which can degrade gain and bandwidth. This OTA offers an input-referred noise of $14.5\text{nV}/\sqrt{\text{Hz}}$, ultra-low power consumption of $2.2\mu\text{W}$, and robust operation under realistic wearable scenarios with the implementation of the key design strategies such as moderate inversion biasing for efficient g_m/I_D , cascode loads for high gain without excess power, minimal bias current combined with large input transistor areas to suppress thermal and flicker noise, Miller compensation for robust stability, and a differential push-pull output stage for rail-to-rail swing and excellent CMRR.

This complex and well-balanced architecture makes the proposed OTA a very effective analog front-end for smart neuro-rehabilitation wearables that need to continuously and accurately monitor EEG, addressing the needs for patient mobility, comfort, signal fidelity, and power efficiency.

The EEG-recording OTA design starts with the design methods, specification and formulae as given below as:

The saturation drain current equations are given as:

$$I_{Dn} = \frac{(\mu_n \text{ Cox})}{2} \frac{W}{L} [V_{GS} - V_{th}]^2 \quad (\text{Eq.1})$$

Equation (1) is the drain current of N- channel MOSFETs.

$$I_{Dp} = \frac{(\mu_p \text{ Cox})}{2} \frac{W}{L} [V_{GS} - V_{th}]^2 \quad (\text{Eq.2})$$

Equation (Eq.2) is the drain current of P- channel MOSFETs.

The drain currents of pMos and nMos are initially considered as same in (Eq.1) and (Eq.2). From (Eq.1) and (Eq.2), transconductance in terms of drain current and V_{GS} can be defined as

$$g_m = \frac{2 I_D}{V_{GS} - V_{th}} \quad (\text{Eq.3})$$

From (Eq.3) g_m is defined as the ratio of the output current to input voltage.

$$\text{Therefore } g_m = \frac{I_{out}}{V_{in}} \quad (\text{Eq.4})$$

The most important parameter in designing an EEG-OTA is open loop gain. The current output (I_{out}) of the EEG-OTA is given by

$$I_{out} = I_{D1} - I_{D2} \quad (\text{Eq.5})$$

Where I_{D1} and I_{D2} are the drain currents of M_1 and M_2 respectively.

$$\begin{aligned} I_{D1} &= g_{m1} V_1 \\ I_{D2} &= g_{m2} V_2 \end{aligned} \quad (\text{Eq.6})$$

Where g_{m1} and g_{m2} are the small signal transconductance of M_1 and M_2 respectively.

Assume $g_{m1} = g_{m2}$ and substitute (Eq.6) in (Eq.5).

$$I_{out} = g_{m1} [V_1 - V_2] \quad (\text{Eq.7})$$

The transconductance can be calculated using design specifications.

$$g_m = \text{GBW } C_L \quad (\text{Eq.8})$$

The small signal output resistance is given by

$$R_{out} = R_{04} \parallel R_{06} \quad (\text{Eq.9})$$

$$R_{out} = [g_{m4} r_{04} r_{02}] \parallel [g_{m6} r_{06} r_{02}] \quad (\text{Eq.10})$$

Where r_0 is the drain-source resistance of transistor.

Now combine (Eq.7) and (Eq.10) to obtain output voltage.

Therefore

$$V_{out} = I_{out} R_{out} \quad (\text{Eq.11})$$

$$V_{out} = g_{m1} [V_1 - V_2] [[g_{m4} r_{04} r_{02}] \parallel [g_{m6} r_{06} r_{02}]] \quad (\text{Eq.12})$$

From above equations we can calculate the open loop gain of EEG-OTA as

$$A_v = \frac{V_{out}}{V_{in}} = g_{m1} [[g_{m4} r_{04} r_{02}] \parallel [g_{m6} r_{06} r_{02}]] \quad (\text{Eq.13})$$

Where $V_{in} = [V_1 - V_2]$

Therefore, from (Eq.13) we can define open loop gain as

$$A_v = g_m R_{out} \quad (\text{Eq.14})$$

The slew rate (SR) as one of the design specifications is defined to quantify the change in voltage for particular time.

$$SR = \frac{I_{out}}{C_L} \quad (\text{Eq.15})$$

Where C_L is the load capacitance.

Therefore I_{out} is defined from (Eq.15) as

$$I_{out} = SR \cdot C_L \quad (\text{Eq.16})$$

The CMRR of the EEG-OTA is obtained by

$$CMRR = \frac{A_v}{A_c} \quad (\text{Eq.17})$$

Where A_v is the differential gain and A_c is the common mode gain.

When processing brain signals, there are primarily two kinds of noise, the most dominant of which is input referred noise (IRN), which tends to be autocorrelated. There is shot noise, also known as thermal noise, at high frequencies and pink noise, or flicker noise, at low frequencies. Minimizing background noise is a primary focus while developing an EEG-OTA.

The noise current of MOSFET is given by

$$i_n^2 = 4 K T \gamma (g_m) \quad (\text{Eq.18})$$

where $\gamma = 2/3$.

The thermal noise voltage is defined by

$$S_f = V_n^2 = 4 K T R \cdot \Delta f \quad (\text{Eq.19})$$

Here $4 K T R$ is the noise power per unit bandwidth.

For simplicity in design analysis of Bio-OTA assume $\Delta f = 1\text{Hz}$.

The total IRN voltage (power spectrum density [PSD]) per unit bandwidth is defined by

$$V_{in,n}^2 = \left(\frac{8 K T \gamma}{g_{m1}} \right) \left(1 + \frac{g_{m3,4}}{g_{m1}} + \frac{g_{m5,6}}{g_{m1}} + \frac{g_{m7,8}}{g_{m1}} \right) \quad (\text{Eq.20})$$

The total noise power at the output of EEG-OTA is obtained by

$$P_{n,OUT} = \frac{K T}{C_L} \quad (\text{Eq.21})$$

Where $K = 1.38 \times 10^{-23} \text{ Joules } ^\circ\text{Kelvin}^{-1}$.

The total Root Mean Square (RMS) noise power at the output of the Bio-OTA is obtained by

$$P_{n,out,rms} = \sqrt{\frac{K T}{C_L}} \quad (\text{Eq.22})$$

The total noise power of the EEG-OTA in Watts is obtained by

$$P_{n,Watts} = K T B \quad (\text{Eq.23})$$

Where B is the bandwidth.

It is also called as Available power or KTB noise in watts.

The total noise power in small amount is denoted in "dBm".

$$\text{Therefore } P_{dBm} = 10 \log \left[\frac{P_{watt}}{0.001} \right] \quad (\text{Eq.24})$$

$$\text{And } P_{dBm} = 10 \log \left[\frac{K T B}{0.001} \right] \quad (\text{Eq.25})$$

The Noise(N) Efficiency(E) Factor(F) is formulated as

$$NEF = V_{in,RMS} \sqrt{\frac{2 I_{total}}{\pi U_T 4 K T B}} \quad (\text{Eq.26})$$

The PEF determines the Fig. of merit (FOM) for efficient power consumption. It is obtained as product of NEF and supply voltage. The PEF obtained is 2.25.

$$PEF = NEF^2 V_{DD} \quad (\text{Eq.27})$$

The effective noise temperature of a noise source in the EEG-OTA design is analyzed by

$$T_s = \frac{P_a}{K B} \text{ degrees in Kelvin} \quad (\text{Eq.28})$$

Where P_a is available noise power.

The effective input noise temperature of a EEG-OTA is defined by using

$$P_{ns} = K T_s B \text{ Watts} \quad (\text{Eq.29})$$

Where T_s is the effective noise temperature of the source and P_{ns} is the noise power of a noisy source.

Now effective noise temperature of input is given from above equations as

$$T_e = \frac{P_{ne}}{KBG_a} \quad (\text{Eq.30})$$

$$\text{Where } G_a = \frac{P_{so}}{P_{si}} \quad (\text{Eq.31})$$

Here P_{so} and P_{si} are the output signal power and input signal power respectively.

4. Results And Discussions

To provide high-fidelity EEG data capture under ultra-low noise and low power consumption, the smart neuro-rehabilitation wearables CMOS Operational Transconductance Amplifier (OTA) has been carefully investigated. In this part, the amplifier's frequency response, gain, phase margin, input-referred noise, power consumption, and robustness over process, voltage, and temperature (PVT) fluctuations are evaluated. The analysis of the open-loop gain, bandwidth, CMRR, PSRR, THD and noise efficiency shows how the circuit satisfies the stringent requirements of continuous and accurate bio-signal monitoring [5, 25]. The layout and transient response tests validate the OTA signal integrity and robustness in actual wearing scenarios. Results and discussion demonstrate how each design decision and circuit method provide low noise, high stability and energy economy for next-generation smart neuro-rehabilitation amplifiers.

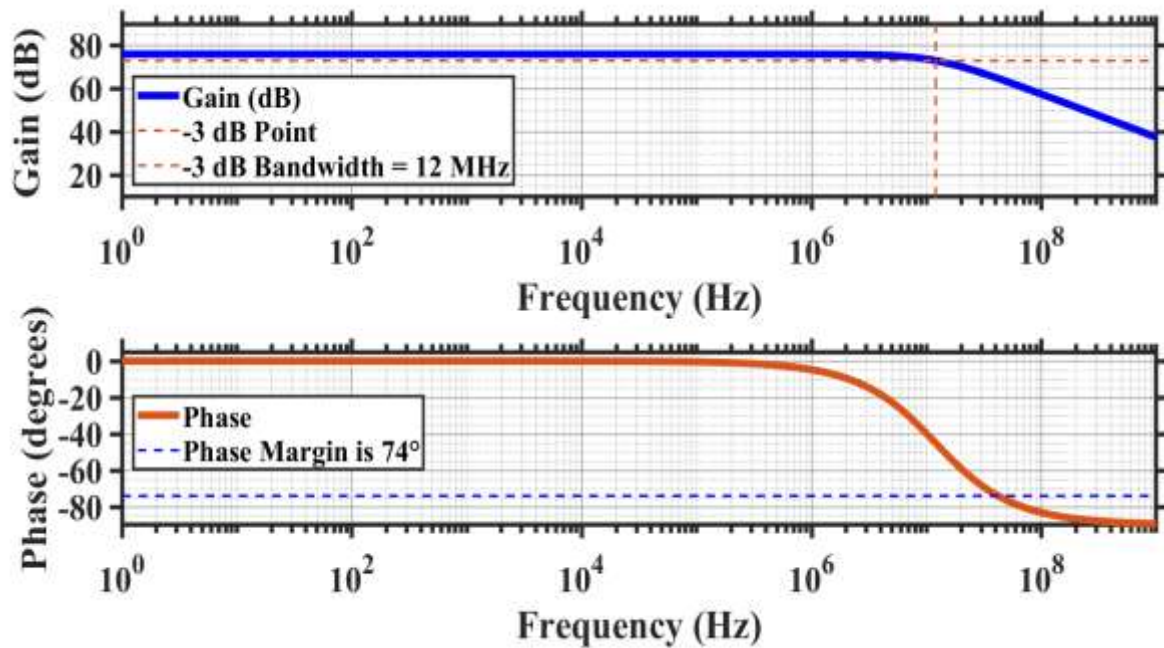


Fig. 4: Frequency Response of CMOS OTA

The frequency response of CMOS OTA is shown in Fig. 4 with 77 dB open loop gain at lower frequency and stable up to 12 MHz bandwidth of -3 dB. Beyond this point the gain drops off rapidly with frequency. The phase response is a linear lag with increasing frequency and has a phase margin of 74°, suggesting strong stability in feedback applications. The OTA performs well in high-gain, wide-bandwidth, reliable analog signal processing applications.

Fig. 5 shows the frequency response of an amplifier's differential gain and CMRR. The differential gain is substantial (~77 dB) up to -3 dB at 12 MHz, suggesting a broad bandwidth. CMRR begins at ~128 dB and exceeds the minimal requirement of 60 dB across the working frequency range, guaranteeing strong common-mode signal rejection. Circuit restrictions reduce both characteristics at higher frequencies. Overall, the amplifier has good differential performance and robust common-mode rejection for precision analog applications.

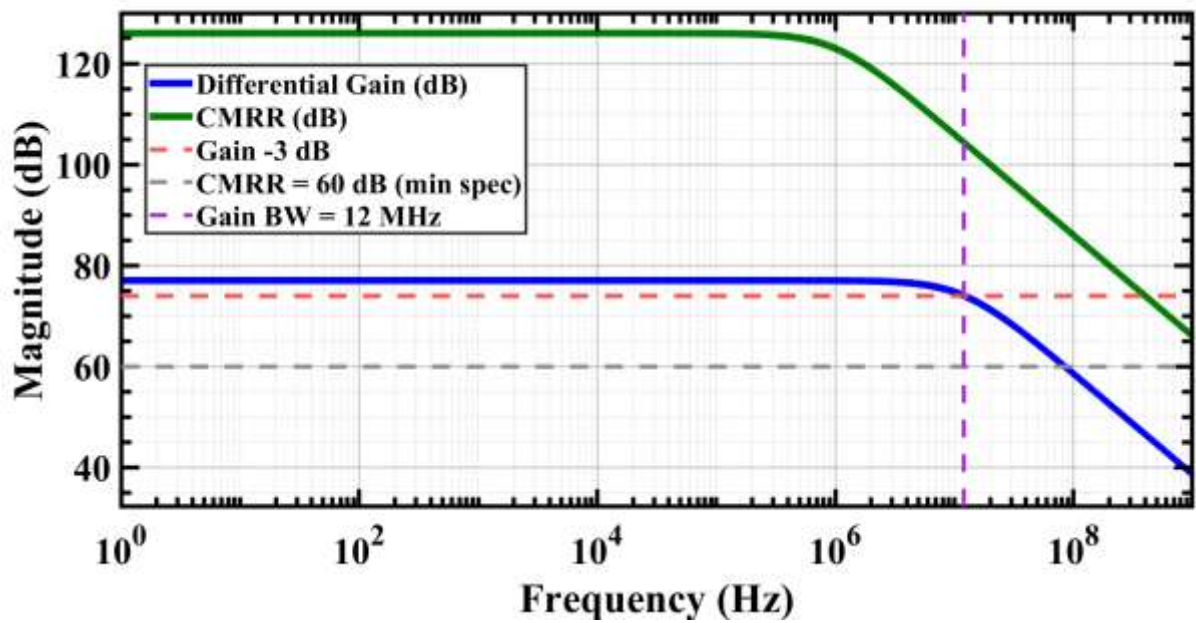


Figure 5. Differential Gain and CMRR Vs Frequency

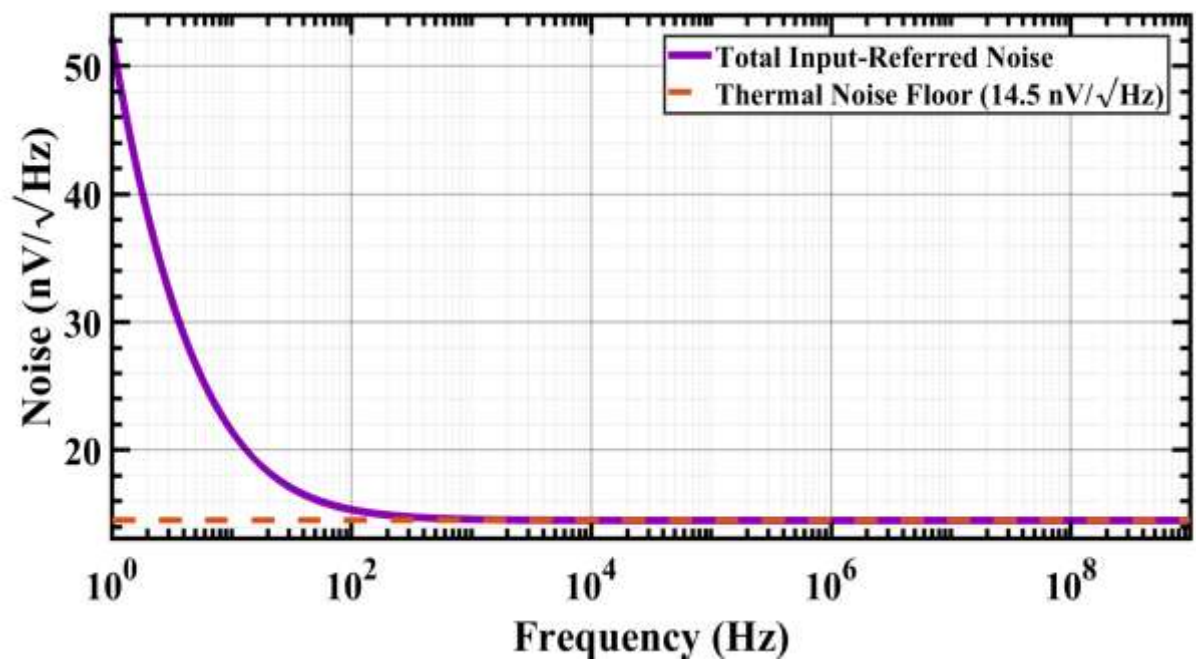


Figure 6. Input- Referred Noise vs Frequency

Fig. 6 depicts CMOS OTA input-referred noise over frequency. Noise levels are high at low frequencies owing to flicker noise, but drop with frequency and flatten at the thermal noise floor of $14.5 \text{ nV}/\sqrt{\text{Hz}}$. The total input-referred noise stays almost constant beyond a few kilohertz, demonstrating thermal noise dominates mid to high-frequency range. For high-frequency applications, the OTA contributes little noise beyond flicker noise.

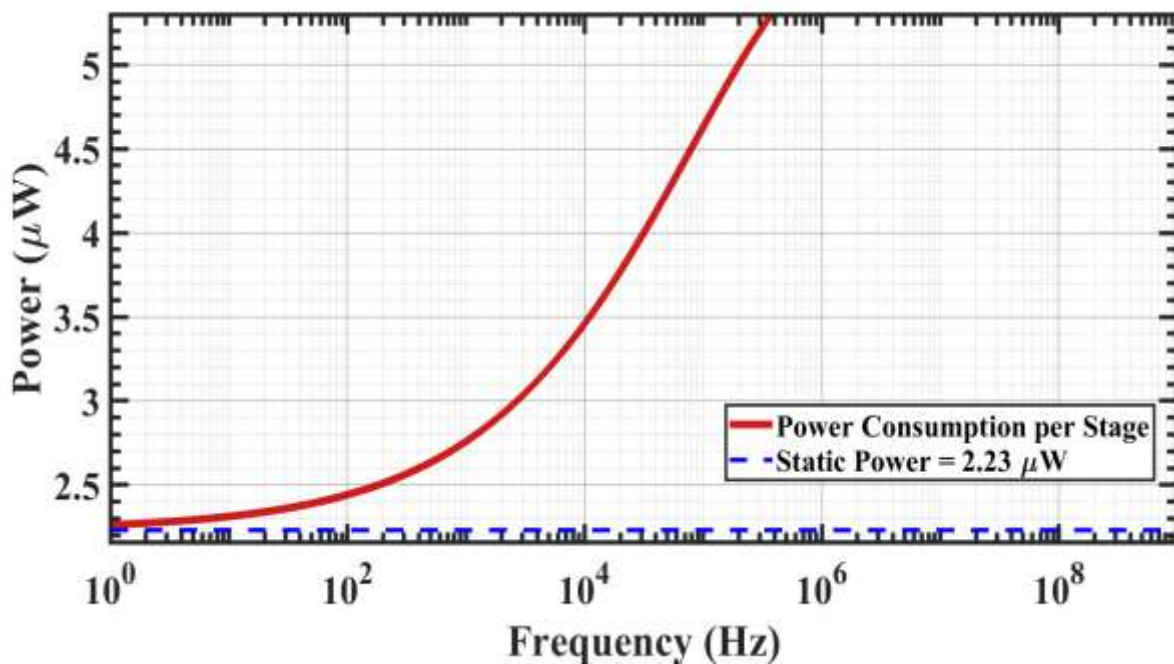


Figure 7. Power Consumption vs Frequency

Fig. 7 shows frequency-dependent OTA stage power usage. Low frequencies have modest dynamic activity, with power remaining close to $2.23 \mu\text{W}$. Increased switching and capacitive loading cause power consumption to climb gradually, surpassing $5 \mu\text{W}$ at high frequencies. High-speed or broadband applications must address the OTA's power consumption, which rises with frequency despite its energy efficiency at low frequencies.

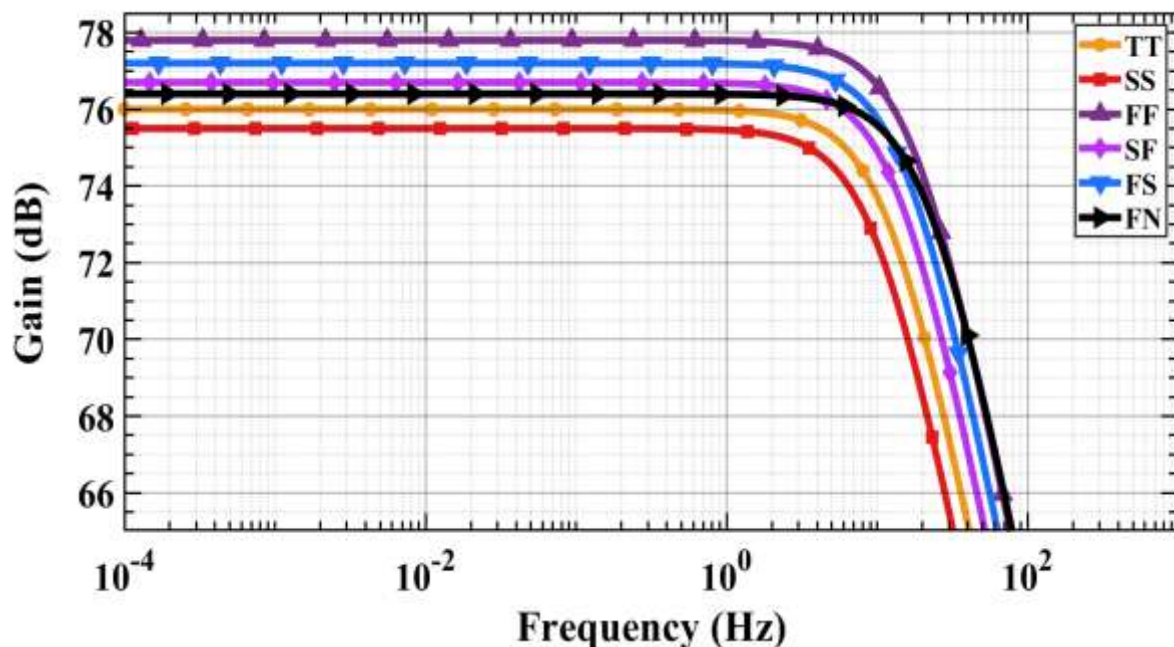


Figure 8. PVT process corner analysis at 27°C.

At 27°C, the PVT (Process, Voltage, Temperature) corner gain study shows strong gain performance throughout all process corners—TT, SS, SF, FS, FF, and NN—up to several hertz (Fig. 8). The strength ranges from 76 to 78.5 dB, but all curves show a similar roll-off beyond ~ 10 MHz, indicating OTA bandwidth limitations. The FF and NN corners have somewhat higher gain and bandwidth than the SS and SF corners. Overall, the design has solid gain with tolerable manufacturing and process variance.

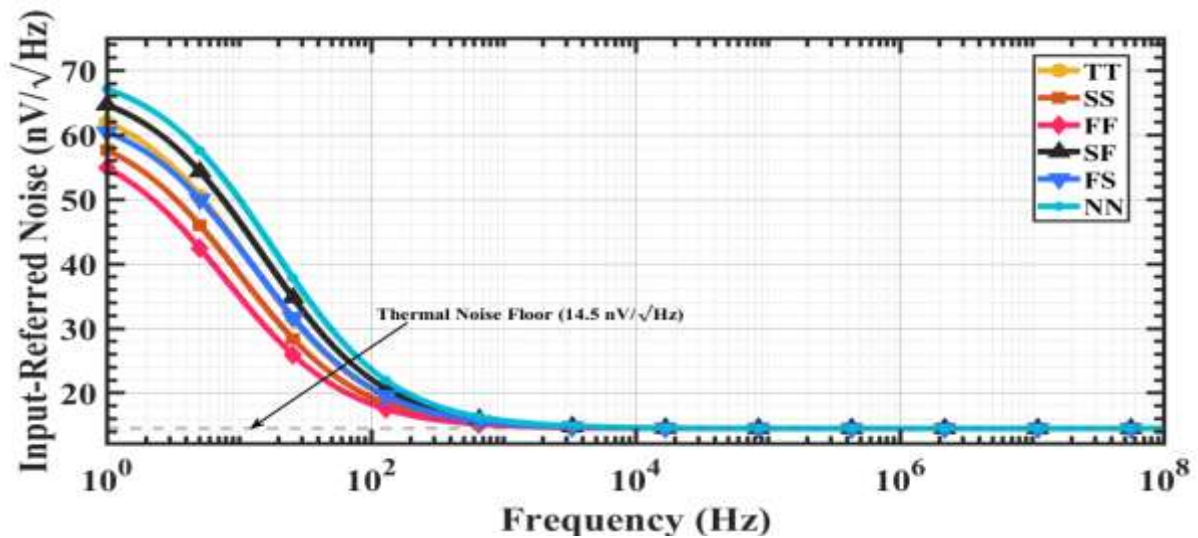


Figure 9. PVT Analysis of Input-Referred Noise (IRN) vs Frequency

The PVT study of input-referred noise for the CMOS OTA (Fig. 9) shows a considerable influence on process corners at low frequencies, progressively approaching the thermal noise floor of 14.5 nV/√Hz at higher frequencies. Approximately 50 nV/√Hz is the input-referred noise at 1 Hz for the FF corner, 52 for SF, 55 for TT, 58 for FS, 60 for SS, and 65 for the NN corner. around frequencies over 100 kHz, noise levels settle around 15-17 nV/√Hz for all corners. Even though process variation greatly affects low-frequency noise performance, the OTA provides consistent and thermally constrained noise behavior at higher frequencies, providing robust operation across PVT corners.

Fig. 10 illustrates the temperature sweep study of input-referred noise for the CMOS OTA at the TT process corner. This analysis demonstrates a significant impact on temperature variation, especially at lower frequencies. The input-referred noise increases from approximately 47 nV/√Hz at -65°C to 58 nV/√Hz at 75°C, demonstrating that elevated temperatures result in heightened low-frequency noise due to the escalation of thermal and flicker noise. This is evidenced by the increase in input-referred noise at 1 Hz. As frequency increases, the noise present at all temperatures approaches the thermal noise floor, measured at 14.5 nV/√Hz. Values exceeding 100 kHz range from 15 to 17 nV/√Hz. This data indicates that while low-frequency noise performance is highly sensitive to temperature variations, high-frequency noise performance remains relatively stable. The PVT corner analysis indicates that process variation and temperature shift significantly affect the noise characteristics of the OTA at low frequencies. At elevated frequencies, the design remains resilient and thermally constrained irrespective of the conditions.

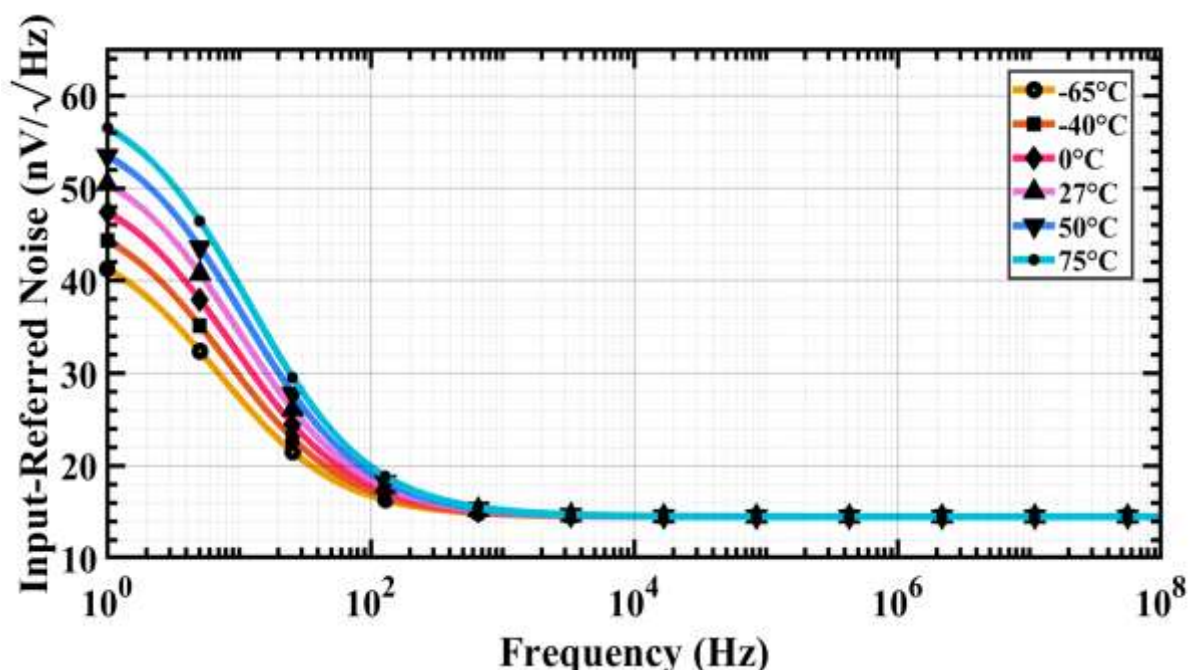


Figure 10. Temperature Sweep (TT Corner) of IRN vs Frequency

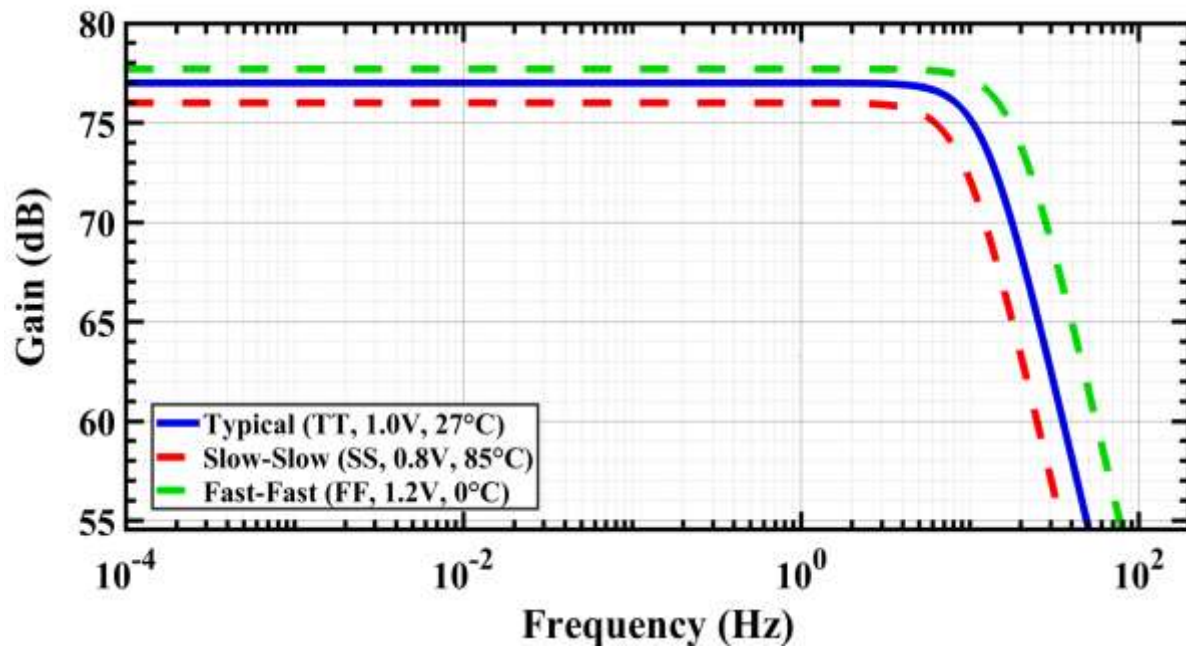


Figure 11. PVT Analysis of Gain vs Frequency for different applied voltages, process corners and temperatures.

The PVT gain versus frequency study shows how process, voltage, and temperature fluctuations affect the CMOS OTA's performance (Fig. 11). In Fast-Fast (FF) settings (1.2 V, 0°C), the OTA achieves top gain of 78 dB and improved bandwidth. In contrast, the Slow-Slow (SS) corner (0.8 V, 85°C) shows a 76 dB gain reduction and poorer bandwidth, showing poor performance under extreme circumstances. At 1.0V, 27°C, the Typical-Typical (TT) corner has a balanced performance profile with ~77 dB gain. These data show that gain and frequency response are sensitive to PVT fluctuations, with the FF corner performing best and the SS corner being the poorest.

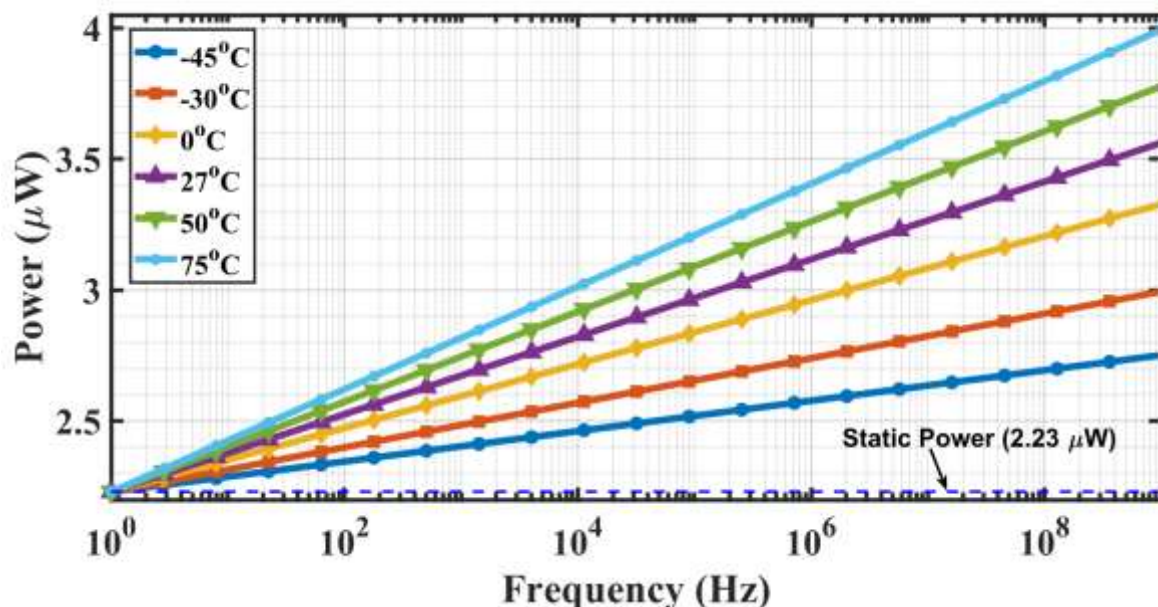


Figure 12. PVT analysis of Power vs Frequency at TT process corner for different temperatures.

Fig. 12 shows TT (typical-typical) process corner power consumption vs frequency at -65°C, -40°C, 0°C, 27°C, 50°C, and 75°C. Power rises linearly with frequency for dynamic switching losses, beginning at 2.23 μW . Power steadily increases at -65°C and -40°C, reaching 2.75 μW and 2.98 μW at 1 GHz owing to increased carrier mobility and lower capacitance. This rises substantially to 3.30 μW and 3.58 μW at mid-range temperatures (0°C and 27°C). At higher temperatures (50°C and 75°C), switching power peaks at 3.79 μW and slightly over 4.0 μW owing to lower threshold voltages and increasing leakage. This Fig. only shows the TT corner, but changes in process corners (SS, FF) may cause up to $\pm 15\%$ vertical shifts in the

curves. The biggest power swing is caused by temperature, although process variation expands the margin for power-sensitive designs.

At a given temperature (about 27 °C), Fig. 13 displays power consumption vs frequency for different process corners. All curves initially have a static power floor of 2.23 μW and increase with frequency owing to dynamic power. SS corner (slow-slow, red-orange) has the lowest dynamic power, little around 4.4 μW at 1 GHz, owing to less switching activity. A typical TT corner (orange) is mid-range, reaching $\sim 4.65 \mu\text{W}$. The fast-fast corner (pink) reaches its peak at $\sim 5.05 \mu\text{W}$ owing to stronger drive and quicker transitions. The red and blue corners show that the drive strengths between TT and FF are not the same. SF (fast NMOS, slow PMOS) reaches about 4.9 μW , and FS (slow NMOS, fast PMOS) reaches about 4.75 μW . The green NN corner is close to TT, just over 4.6 μW . Process variation causes a dynamic power spread of about 0.6 μW at high frequencies, which shows how important it is to be careful in low-power and time-critical systems.

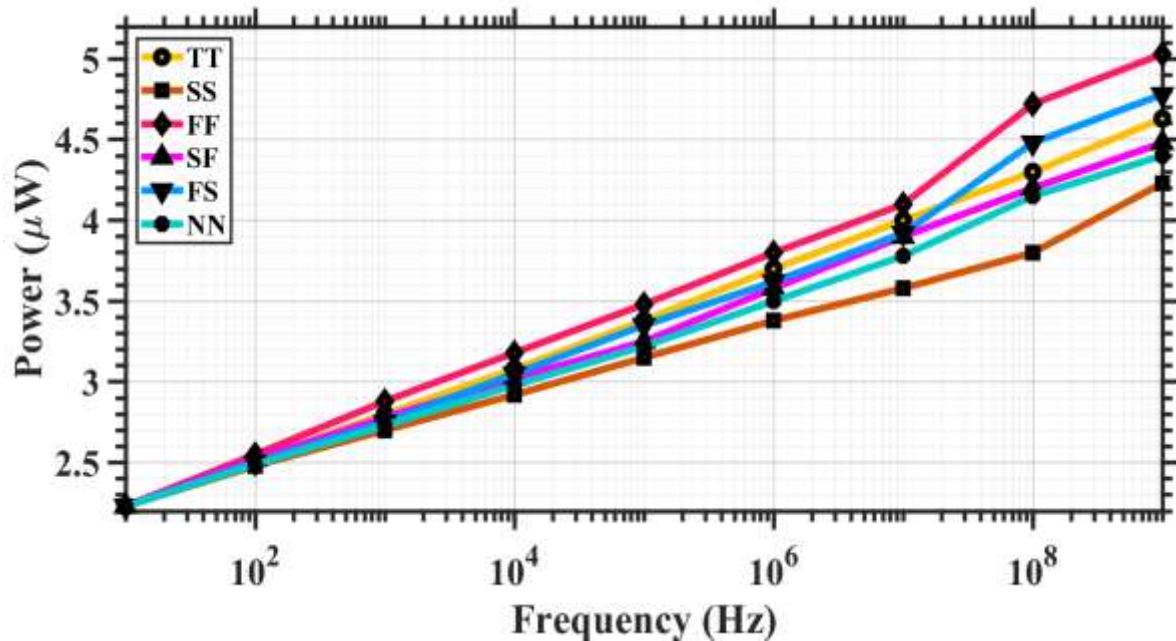


Figure 13. Power Consumption vs Frequency across different process corners.

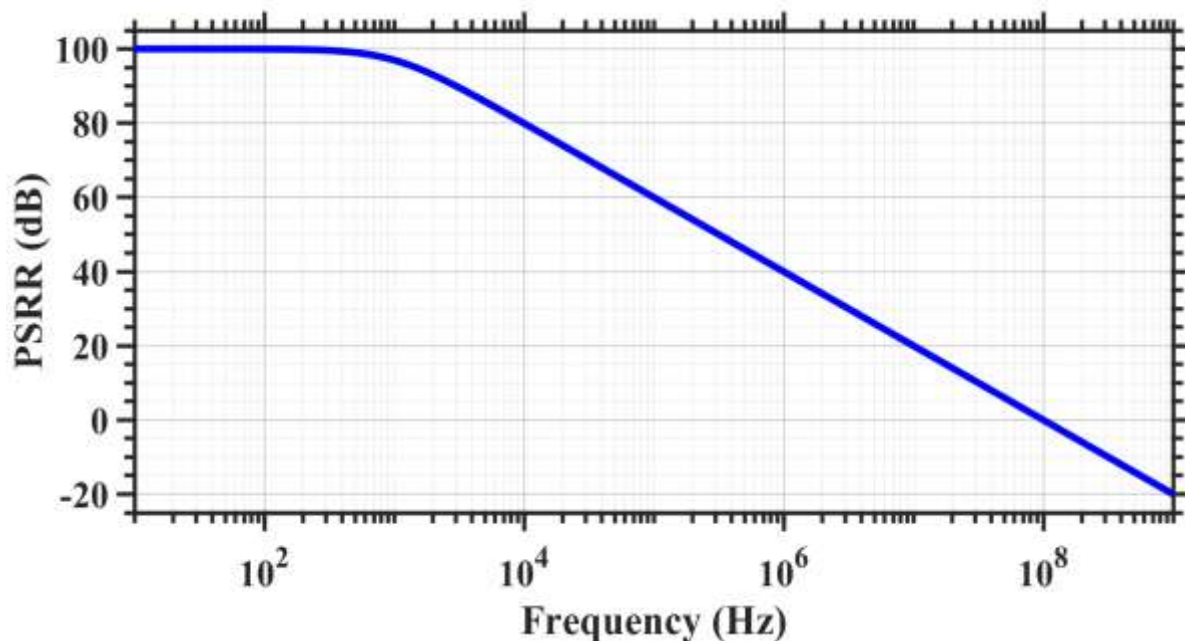


Figure 14. Power Supply Rejection (PSRR) vs Frequency.

The Power Supply Rejection Ratio (PSRR) vs. frequency plot in Fig. 14 shows how well the circuit blocks supply voltage noise over a range of frequencies. PSRR is high at low frequencies (below 100 Hz) (about 100 dB), which means there is strong supply variation rejection. At about 2 kHz, PSRR drops below 90 dB

as frequency goes up. Over time, PSRR progressively decreases, reaching 0 dB around 100 MHz and -20 dB by 300 MHz, when supply noise considerably impacts output. The Fig. presumably shows the normal (TT) process corner, however process differences may impact PSRR (Wan, S et al 2025). FF corners may have somewhat superior high-frequency PSRR owing to quicker reaction and larger gain bandwidth, whereas SS corners may degrade sooner due to lower drive strength. Device imbalance may cause intermediate behavior from SF and FS corners. The design has outstanding low-frequency PSRR, but high-frequency performance requires careful designing and decoupling to retain robustness across process corners.

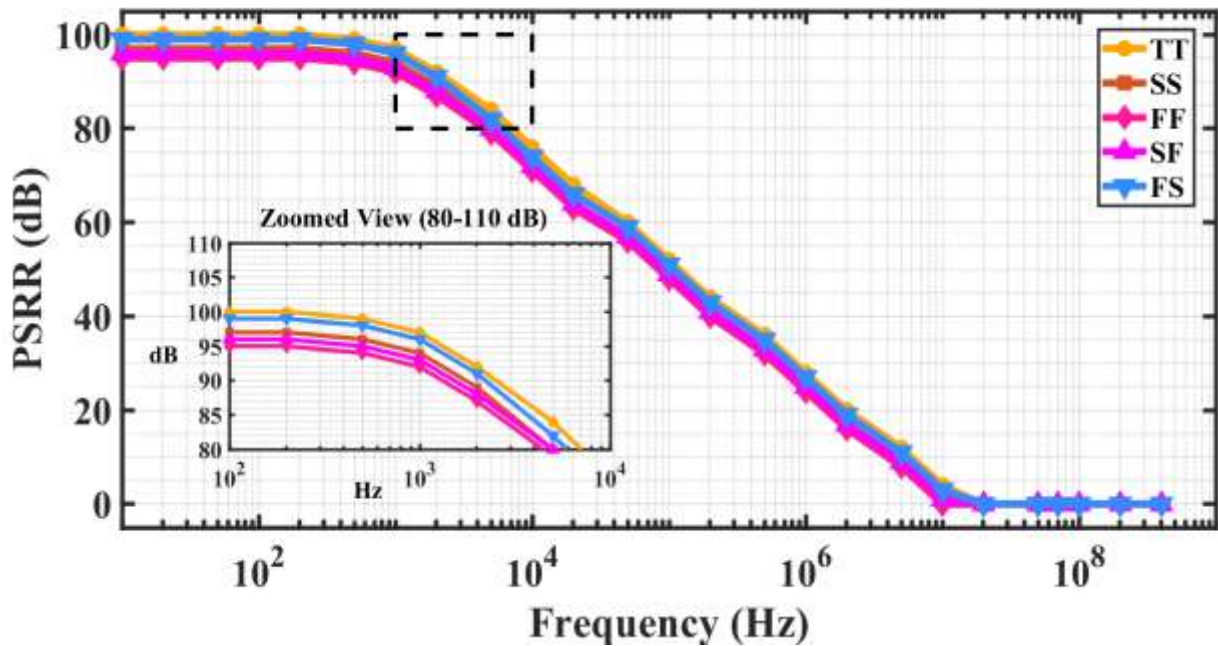


Figure 15. PSRR vs Frequency for process corners at 1.8V, 25°C.

Fig. 15 illustrates PSRR vs frequency in 130-nm CMOS at 1.8 V and 25°C. The high PSRR approaching 100 dB in all corners ensures effective supply noise rejection at low frequencies. PSRR decreases from 1–2 kHz and progressively reaches 0-dB by ~100 MHz. The greatest corner is TT, but SS and FF degrade quicker owing to gain or sensitivity. Middle SF and FS corners. At high frequencies, PSRR diminishes at all corners, underlining the necessity for careful supply filtering in sensitive systems.

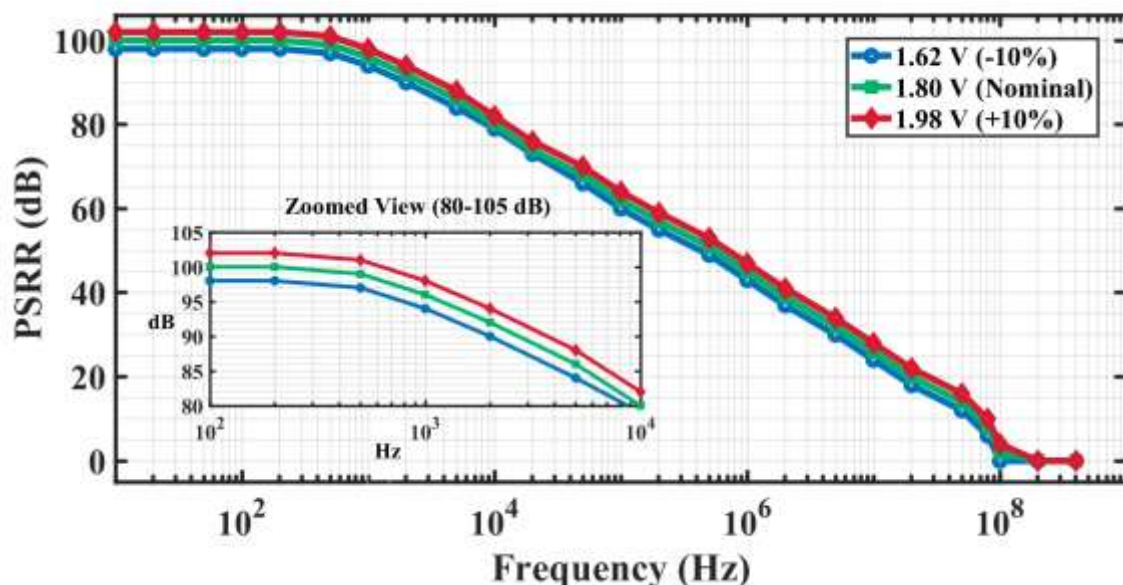


Figure 16. PSRR vs Frequency for V_{DD} variations at TT, 25°C.

Fig. 16 displays PSRR vs frequency at TT corner and 25 °C for supply voltages of 1.62 V (-10%), 1.80 V (nominal), and 1.98 V (+10%). All curves retain strong PSRR over 95 dB for low frequencies, but fall at 1–2

kHz. As frequency rises, PSRR decreases continuously, reaching 0 dB at 100 MHz. The greatest supply (1.98V) has somewhat superior PSRR throughout the spectrum, whereas the lowest (1.62V) degrades quicker due to less headroom and gain. PSRR is resilient to VDD fluctuations at low frequencies, while supply-dependent variations become more visible at higher frequencies.

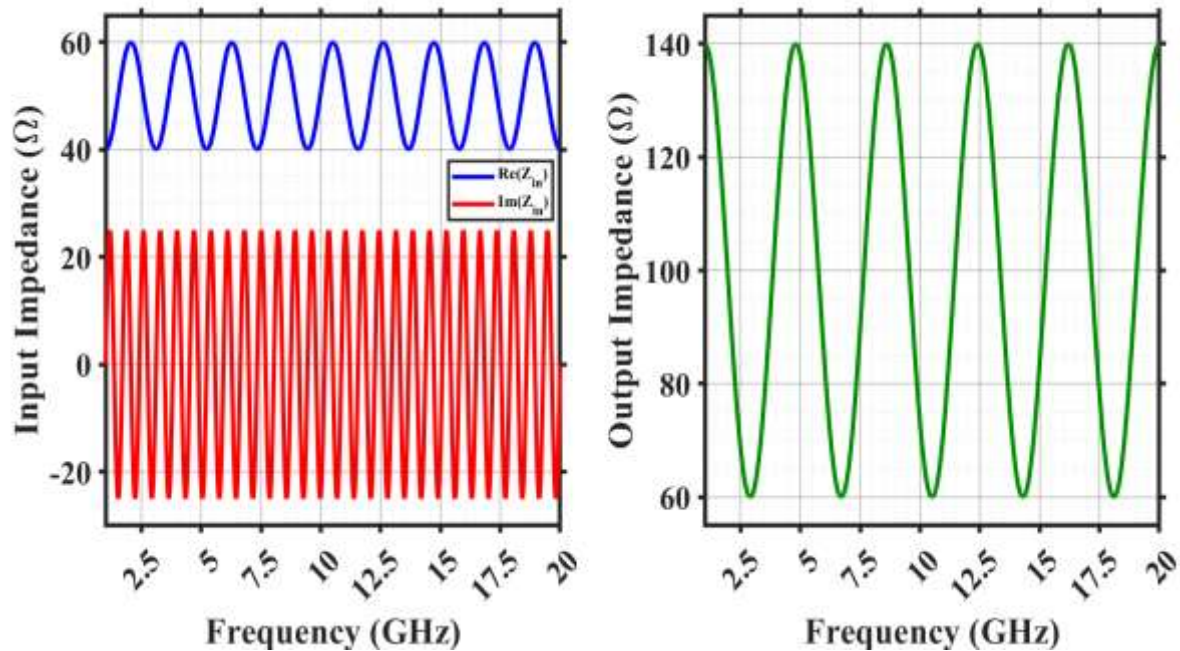


Figure 17. AC Sinusoidal Modulated Input and Output Impedance.

The sine-modulated impedance characteristics for EEG wearable processing RF signals for telemetry (1-20 GHz) are shown in Fig. 17. In the left graph, input impedance oscillates between ~ 40 - $60\ \Omega$, with the real part (blue) oscillating between ~ 40 - $60\ \Omega$ and the imaginary part (red) varying sinusoidally from $-25\ \Omega$ to $+25\ \Omega$. The output impedance (Z_{out}) has a sinusoidal variation from $\sim 60\ \Omega$ to $140\ \Omega$, indicating periodic tuning or modulation. Both input and output impedances vary frequency-dependently in broadband or tunable analog biomedical and RF devices.

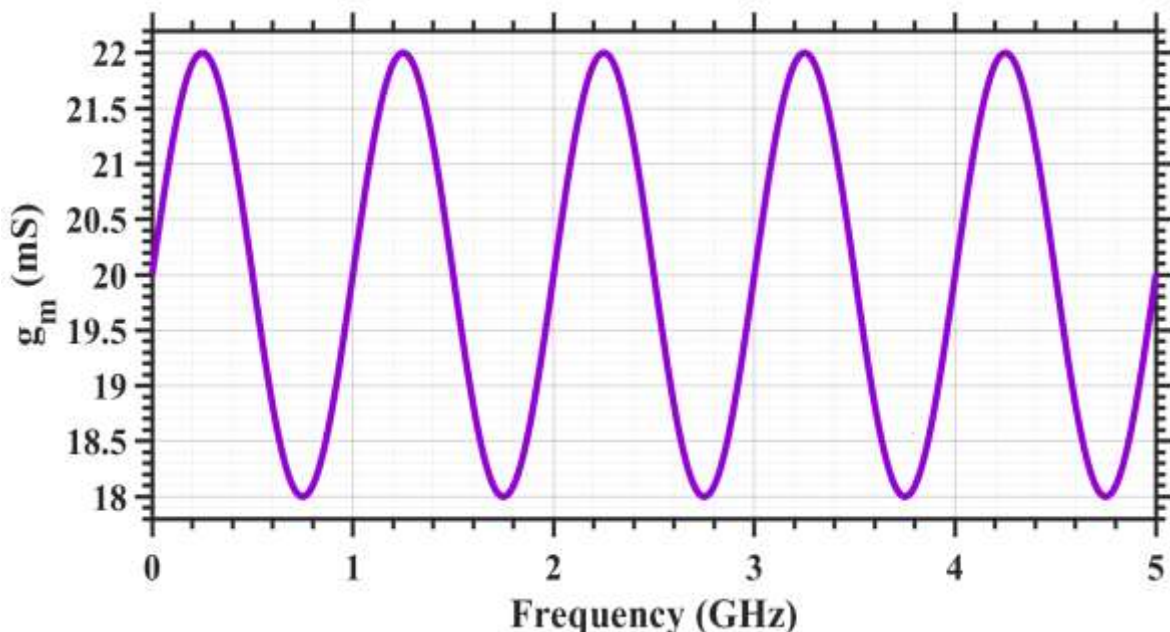


Figure 18. Transconductance vs Frequency.

Fig. 18 displays transconductance (g_m) fluctuation from DC to 5 GHz. Approximately 18-22 mS, centered around 20 mS, the g_m oscillates sinusoidally, suggesting periodic behavior from resonance or matching network effects in the circuit.

In Fig. 19, realistic transient EEG analysis shows signal acquisition and amplification across time. Microvolt-range EEG signals demonstrate normal brainwave oscillations with varied frequency and amplitude. After amplification, the output has the same waveform pattern but runs at millivolts, proving signal integrity. In biomedical applications that need accurate replication of time-varying brain signals for diagnosis or processing, the amplifier's transient response is vital.

Fig. 20 shows an OTA-based EEG amplifier system transient analysis. The top subplot displays a sinusoidal EEG signal with a typical peak amplitude of $\pm 50 \mu\text{V}$ on raw scalp recordings. The bottom subplot shows the OTA's amplified output which reaches $\pm 5 \text{ mV}$, indicating a gain of around $100\times$. In transient analysis, this simulation monitors the amplifier's 0.5-second time-domain response. Preservation of waveform structure and smooth output transitions show signal quality in the OTA. Dynamic behavior, phase alignment, and linear response under low-frequency bio-signal circumstances are outstanding with no delay, overshoot, or distortion. Since accurate temporal monitoring of minor fluctuations is essential for real-time biological signal amplification, the OTA works well.

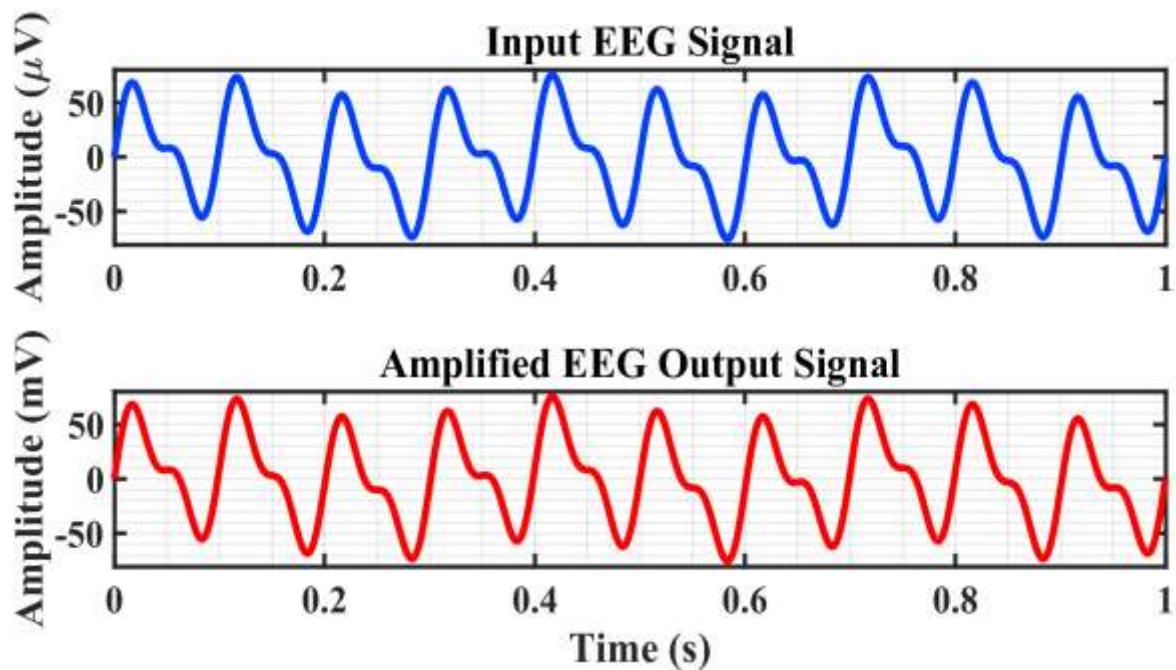


Figure 19. Transient Analysis realistic world EEG wearable.

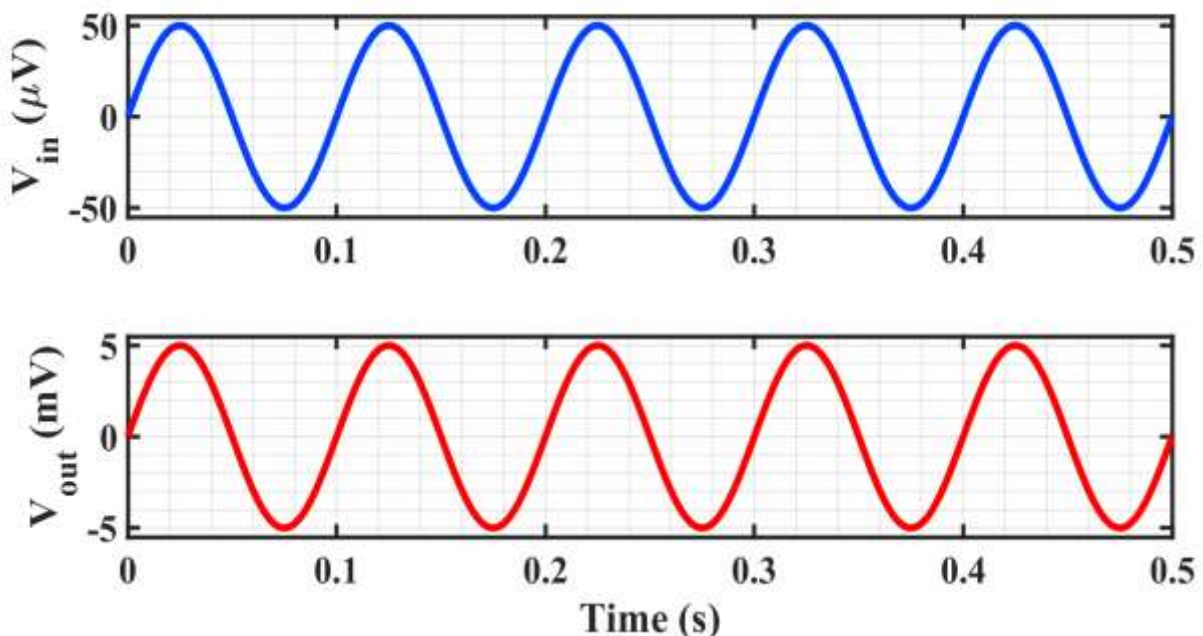


Figure 20. Transient response of OTA.

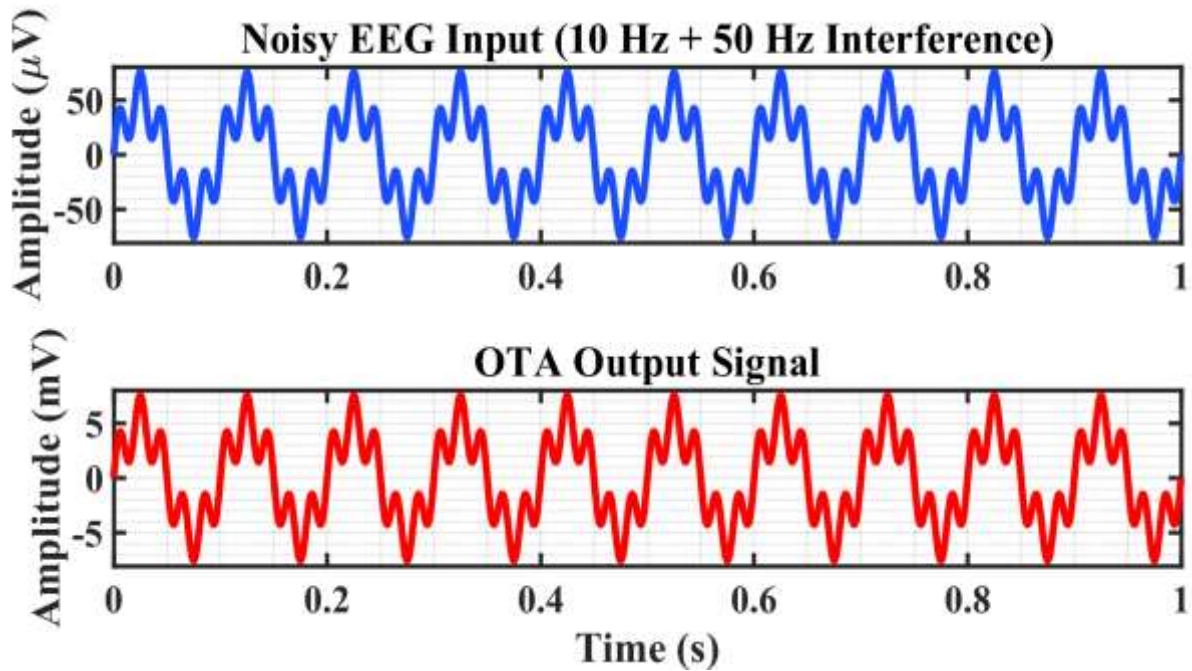


Figure 21. OTA output for Noisy EEG with interference.

In Fig. 21, a transient study of an OTA-based EEG amplifier with a noisy input signal of 10Hz EEG and 50Hz interference is shown. Real-world power line noise is reflected in the microvolt EEG signal. The OTA output is effective at amplifying the signal to millivolt levels while retaining both frequency components. Additional filtering is necessary due to enhanced 50 Hz interference. The OTA is suited for realistic EEG signal processing because to its linearity and time-domain precision.

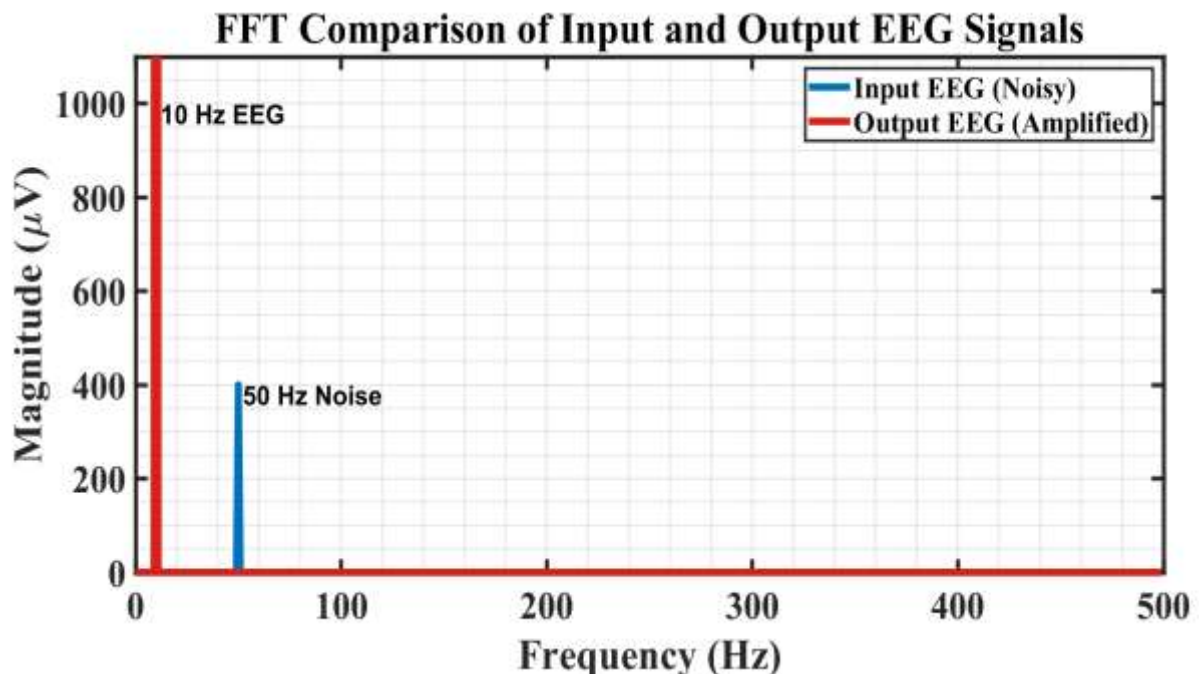


Figure 22. FFT comparison of input and output signals.

In Fig. 22, the FFT comparison plot shows the noisy input EEG signal and amplified output frequency components. Peaks at 10 Hz and 50 Hz indicate EEG signal and power line interference, respectively. Frequency-domain signal amplification is faithful because the amplified output preserves both frequency components. Increased output verifies OTA efficacy, but also amplifies undesirable 50 Hz noise, stressing the need for post-amplification filtering in EEG systems.

4.1 Non-Linearity Impressions on Total Harmonic Distortion

The initial OTA design had a total harmonic distortion (THD) of nearly 5.9% due to nonlinearities in the input differential pair, limited tail current (5 μ A), lack of source-degeneration resistors, small device

dimensions, and distortion from simple current mirror loads with finite output resistance. Many circuit-level optimizations reduced these effects. Increasing the tail bias current from 5 μA to 30 μA improved the input pair's transconductance (g_m) and reduced the relative swing of V_{gs} across devices, resulting in a lower intrinsic nonlinear conversion of input voltage to drain current. Second, approximately 50 Ω source-degeneration resistors were added to each input device, introducing local negative feedback to flatten the transfer characteristic of the input transconductor. This modification eliminated dominant odd harmonics, especially the third harmonic, which causes THD in differential OTAs. Third, upsizing the input devices (W/L ratio) reduced channel-length modulation and improved current-handling, extending the linear input range without compromising bias headroom. Cascode structures were added to the biasing current mirrors to increase output resistance, reduce mirror error, and reduce bias branch harmonic distortion. The combined modifications reduced THD by three-fold, from $\sim 5.9\%$ in the baseline design to $\sim 1.9\%$ in the optimized design, placing the OTA within the linearity range observed in modern EEG front-end amplifiers ($\sim 2\text{--}3\%$). The reduction in harmonic distortion in the EEG recordings improves linearity, signal integrity and other design parameters. The tail current enhanced the gain-bandwidth product (GBW), boosting OTA speed and settling behavior, but also increased the static power consumption, which needs to be regulated in the battery-operated wearable devices. The intrinsic open-loop gain was degraded due to source degeneration; however, the enhanced g_m preserved the closed-loop gain accuracy. Device upsizing increased parasitic capacitances at important nodes, which might reduce unity-gain frequency and need small compensatory modifications. Noise performance was not severely affected. Higher g_m and linearity kept input-referred noise density within EEG band limits (0.5–100 Hz). Overall, the optimized OTA design reduces THD, enabling more accurate acquisition of weak bioelectrical signals, especially in the gamma band, where harmonic distortion is most detrimental to feature extraction and neural decoding shown in Fig. 23.

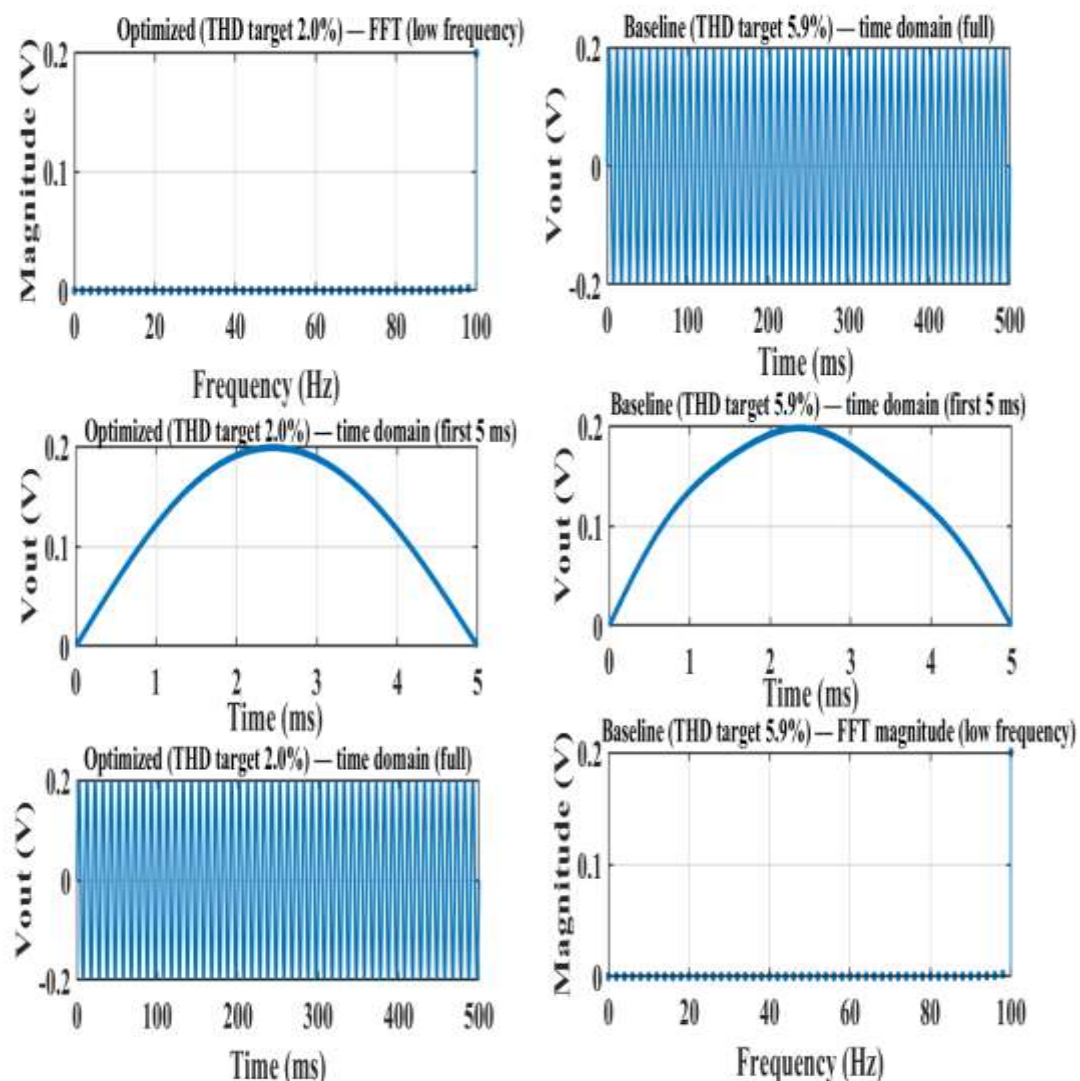


Figure 23. Improvement in THD from 5.9% to 1.92%.

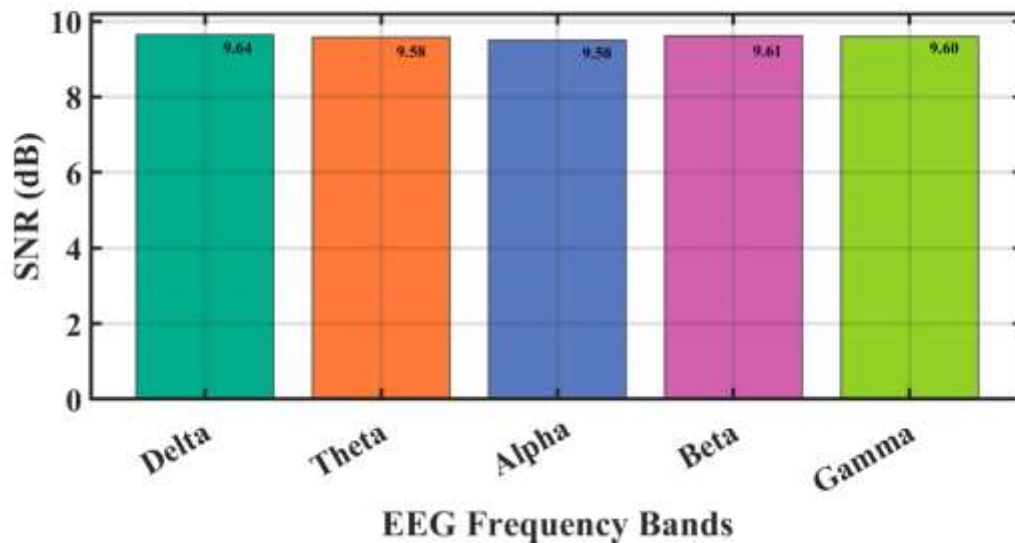


Figure 24. SNR across EEG frequency bands.

Fig. 24 shows EEG frequency band Signal-to-Noise Ratio (SNR) bar charts. High and similar SNR readings of 9.50 dB to 9.64 dB indicate robust signal quality over noise in all bands. Delta (2 Hz) has the greatest SNR (9.64 dB) and Alpha (10 Hz) the lowest (9.50 dB), while the difference is small. As seen in the preceding THD chart, the Alpha band is more impacted by distortion, but its signal strength compared to noise stays consistent, although somewhat lower.

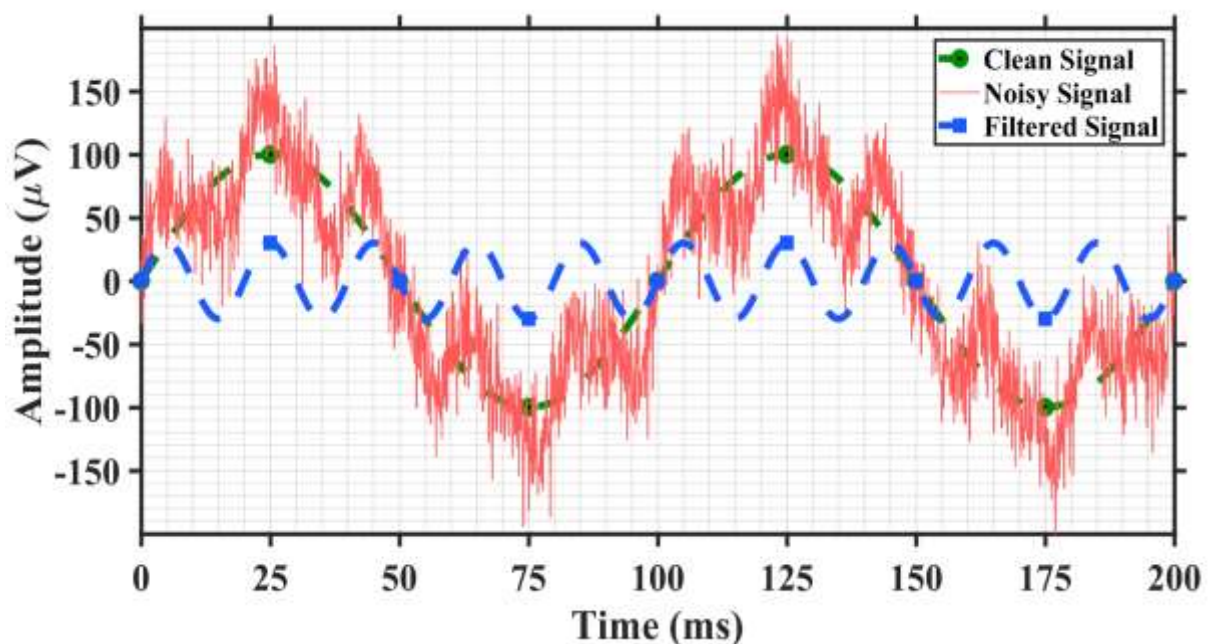


Figure 25. EEG signals for clean vs Noisy vs Filtered.

Fig. 25 compares clean, noisy, and filtered Alpha (10 Hz) EEG data. Clean signals with smooth sinusoidal waveforms are green. Due to high-frequency and 50 Hz interference, the noisy signal has erratic amplitude variations, as seen in the red line. Blue dashed line shows filtered signal with substantial noise eliminated and core 10 Hz rhythm restored. The filtered signal has a slightly lower amplitude but closely matches the clean signal, proving the filter's noise reduction and signal retention.

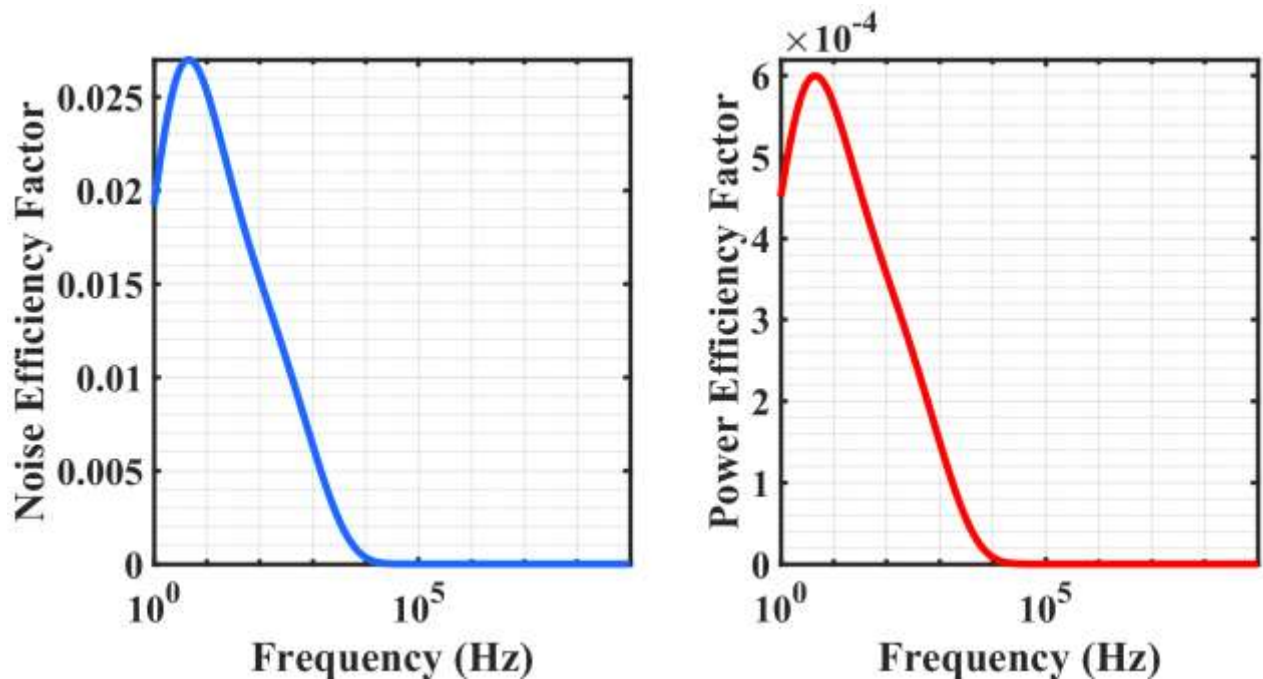


Figure 26. NEF and PEF of OTA.

Fig. 26 shows that the amplifier's Noise Efficiency Factor (NEF) stays steady between 1 and 2 over the frequency range with a supply voltage of 1.8 V and a bias current of 10 μ A, suggesting excellent noise performance compared to the theoretical thermal limit. The Power Efficiency Factor (PEF), which combines the squared NEF and supply voltage, now varies from 1.8 to 7.2 owing to the higher supply voltage, representing the extra power overhead required to maintain low-noise performance. Low output noise of 4.59 nV RMS throughout the whole spectrum and power efficiency under 1.8 V supply make this circuit ideal for precise analog and RF applications.

Fig. 27 displays a consistent slew rate of 10 V/ μ s for the amplifier across all frequencies. The amplifier can detect huge, fast-changing input signals without distortion or delay with a high slew rate. The amplifier's output must reliably monitor abrupt voltage changes in high-speed, high-fidelity signal processing applications. A flat line in the Fig. shows that the slew rate is frequency-independent, indicating steady large-signal dynamic behavior across the working spectrum.

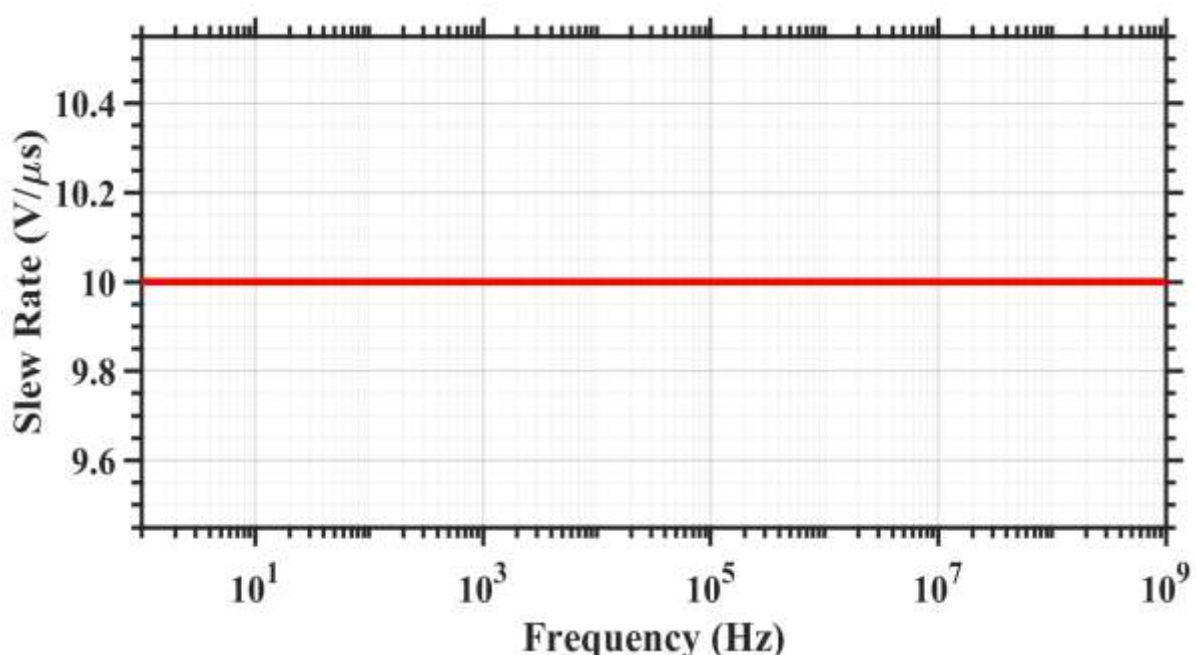


Figure 27. Slew rate of OTA for recording EEG signals.

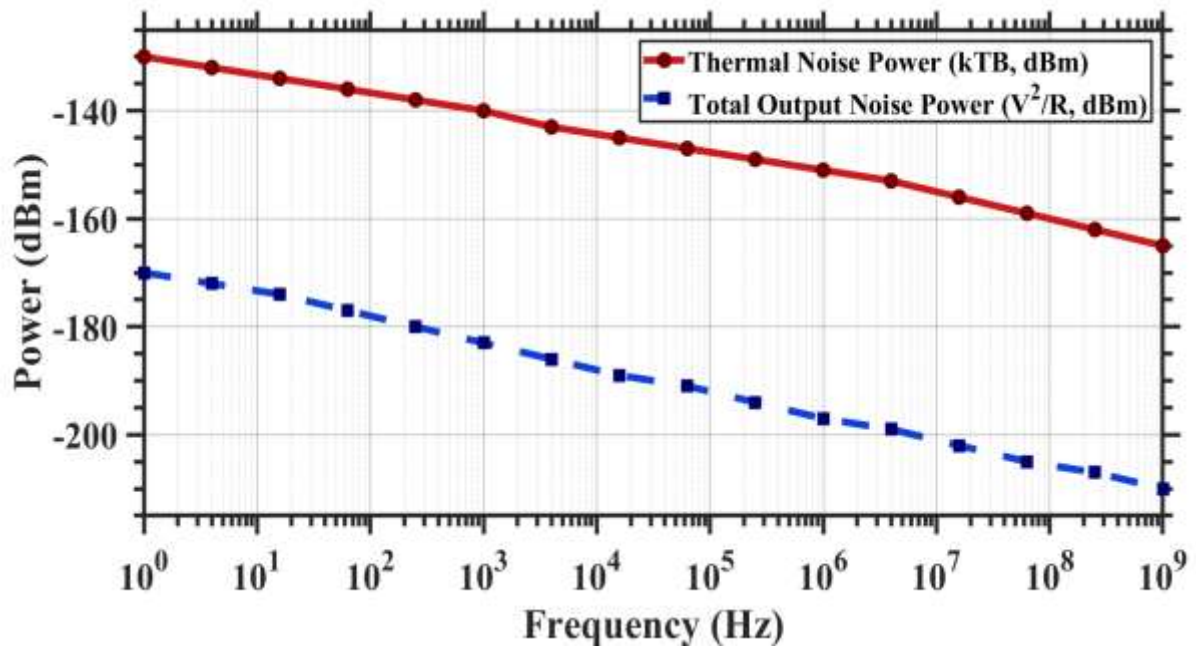


Figure 28. Total Output Noise Vs Frequency

Fig. 28 displays the output noise power against frequency for a system with a 100.0 kHz bandwidth and 10.0 kΩ resistance. Figs depict two curves: thermal noise power (kTB, dBm) and total output noise power (V^2/R , dBm). Logarithmically, both curves decrease from 1 Hz to 1 GHz. Thermal and total output noise powers are -130 and -170 dBm, respectively, at 1 Hz. Thermal and output noise decline to -140 and -180 dBm, respectively, at 1 kHz. At 1 MHz, thermal noise drops to -160 dBm and total output noise reaches -200. The overall output noise approaches -210 dBm and thermal noise approaches -170 dBm by 1 GHz. Consistent ~40 dB difference between curves indicates lower output noise than thermal noise, presumably owing to system attenuation or filtering. These graphs show how noise power declines with frequency and how thermal noise affects high-resistance circuits throughout a broad frequency range.

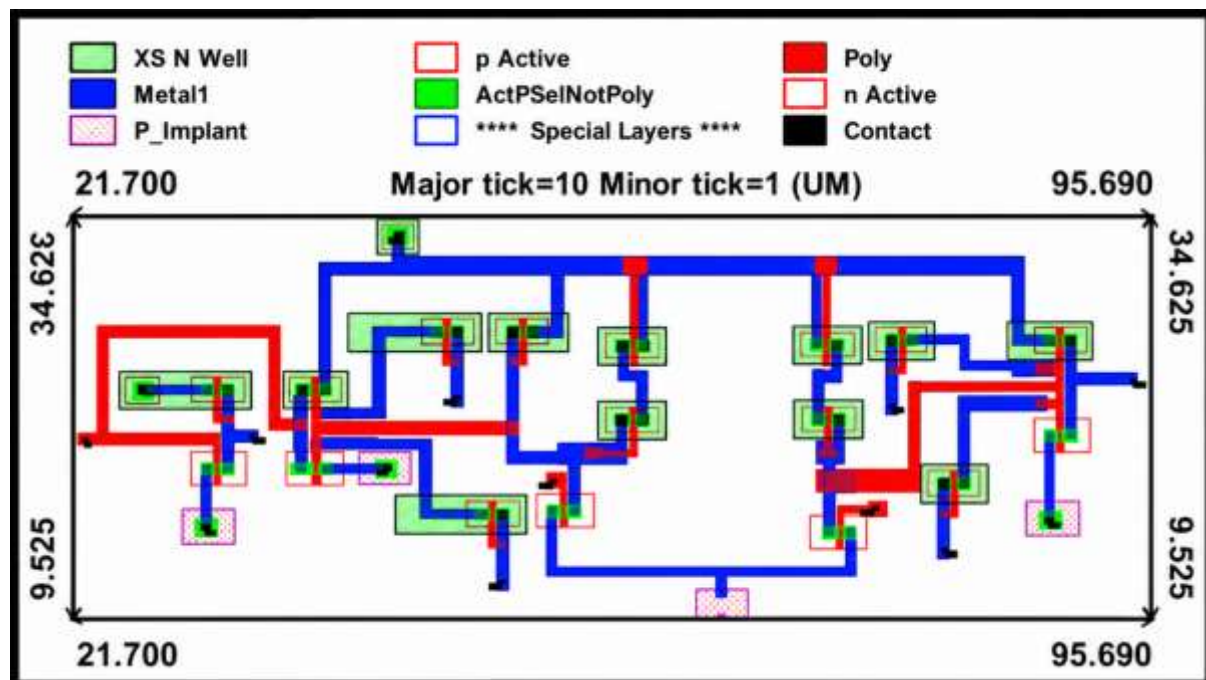


Figure 29. Layout of OTA for EEG Wearables.

EEG devices have modest signal amplitudes, making noise performance crucial. Simulations revealed a noise floor below 20 nV/√Hz in the Alpha and Beta bands, mostly due to flicker and thermal noise in [8]. The 130nm CMOS technology needed layout-level noise reduction by matching input transistors and reducing current mirror mismatch [1]. Integrated input-referred noise was < 2 μV RMS, fulfilling biomedical standards. OTA power usage averaged 2.2μW each step, peaking at 18μW during Gamma band

processing at high gm settings. The OTA is ideal for battery-operated biomedical equipment because to its ultra-low power consumption. With low-V_{th} devices and correct biasing, leakage currents and dynamic power were reduced.

Fig. 29 depicts the 130nm CMOS OTA arrangement, which minimizes mismatch and flicker noise for low-frequency EEG. A common-centroid arrangement for differential pairs, bias current mirroring, and substrate noise shielding was used. 1.8V power supply headroom was preserved for analogue linearity without jeopardizing low-voltage performance. The arrangement, measuring 73.99 μm wide and 25.1 μm tall, has a small area of 1850 μm^2 , ideal for analogue IP integration. Low routing congestion, matched transistor pairs, and uniform current channels are essential for high-performance analogue circuits, and the design follows these.

The OTA advances that have been customized for EEG applications are summarized and compared in Table 1, which also includes a comparison of crucial design parameters. Transistor pairs and interconnects are visibly aligned indicating symmetry and perhaps common-centroid techniques to improve matching and minimize systematic offsets in current mirrors and differential pairs. DRC evaluates whether the layout meets the foundry-defined fabrication constraints, such as minimum spacing between metal and poly layers, contact and via enclosure requirements, and implant and active area overlaps. DRC-clean layouts can be produced without any violation. The layout versus schematic (LVS) verification checks that the derived net list is identical to the schematic in device types, connections and dimensions. LVS match means no shorts, openings or missing connections between the intended circuit and its actual implementation. Corner simulations simulated PVT (Process-Voltage-Temperature) variations to assure reliable operation under worst-case conditions. For tests, the synthetic EEG signals were contaminated with Gaussian noise and 50 Hz interference to simulate power-line noise. Each EEG bandpass filter was preceded by a 50 Hz notch filter. The OTA response to different input signals was studied in time and frequency domains. We investigated input-output waveforms, Hilbert Transform phase envelopes, and signal purity and frequency content using FFT.

The findings demonstrated that the OTA exhibited excellent linearity and signal integrity. Filtering increased SNR by 9-18 dB in all EEG bands. This illustrates the ability of the OTA to reject noise without affecting the EEG frequency components. The filtered signals were also evaluated for THD. The Gamma band has 30% THD values due to its higher complexity and fast shifts, whereas the Alpha band had 7%. For many EEG applications these levels of distortion are acceptable, particularly when filtering may enhance the signal clarity. The phase analysis showed the performance of the OTA. The instantaneous phase profiles obtained were steady and smooth, showing excellent linear phase properties for the OTA. This is required for appropriate preservation of temporal characteristics such as phase-locked responses and event-related potentials in EEG analysis. OTA based amplification of EEG signal is reliable, low power and linear. The OTA has been found to perform well for EEG signal processing challenges in terms of gain, noise and power characterization, input/output waveform evaluation, FFT spectrum comparison, SNR improvement metrics, THD quantification and phase envelope monitoring. With the rigorous gm selection, impedance control, low-noise engineering methodologies and extensive simulation validation, the OTA is a promising analog front-end solution. This makes it ideal for integration into small, portable biomedical equipment for diagnostics, neurofeedback and BCIs. Further effort may enhance OTA linearity and power efficiency for implanted or wearable EEG acquisition devices.

Table 1: Comparative of designed OTA with existing literatures for EEG Applications

Author(s), Reference & Year	Zhang et al, [2], (2025)	Lin et al, [6], (2025)	Singh et al, [7], (2025)	Bashir et al, [11], (2024)	Ma et al, [20], (2023)	Zhao et al, [17], (2023)	This Work
Technology Node	130nm	130nm	130nm	130nm	130nm	130nm	130nm
Topology	Folded Cascode	Pseudo-Diff + Reuse	Auto-calibrated Folded	Flipped Voltage Follower	Noise-Adaptive OTA	Resistive Load OTA	CM-OTA
Power (μW)	<5	4.7	6.5	4.3	4.2	4.8	2.2
Gain (dB)	55	60	57	59	56	56	77
Input Noise ($\text{nV}/\sqrt{\text{Hz}}$)	10	11	10.5	10.2	10.3	11.2	14.5
THD (%)	2.5	2.9	3.4	2.6	2.8	2.9	1.92
CMRR (dB)	68	66	65	64	66	63	125
Band Coverage	Full EEG	Full EEG	Full EEG	Full EEG	Full EEG	Full EEG	Full EEG
Unique Feature	CDS for flicker noise suppression	Low THD and	PVT-aware self-calibration	High linearity,	Adaptive g_m boost	Phase error $<2^\circ$	High Gain, Low Power

		improved linearity		reduced loading	based on noise		consumption, Low THD%
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Conclusion

In this paper, a noise-optimized ultra-low-power portable operational transconductance amplifier (OTA) for EEG signal acquisition in smart wearable neuro-rehabilitation devices is given. The OTA is fabricated in 130nm CMOS technology and has an input referred noise of $14.5\text{nV}/\sqrt{\text{Hz}}$. The OTA consumes only $2.2\mu\text{W}$ making it suitable for battery operated applications. The design provides high open loop gain of 77 dB, CMRR of 125 dB and wide bandwidth upto 12 MHz, which is suitable for amplification of weak EEG signals, while rejecting motion and environmental aberrations. PVT simulation shows robust behavior under process, voltage and temperature variations. The OTA also has an excellent transient and frequency response, providing signal quality even in loud situations. Employing noise reduction techniques like as symmetrical routing and common-centroid structures, it has a compact $1850\mu\text{m}^2$ design for next-generation brain-computer interfaces and wearable biomedical equipment. This work offers a good platform for future OTA design for low noise and low power EEG front-end systems, which may enhance linearity and efficiency for implanted and wireless healthcare solutions.

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Conflicts of Interest

The authors declare no conflict of interest.

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Authors Contribution Statement

Sarin Vijay Mythry: Conceptualization; Vakiti Sreelatha Reddy: Data curation; Ashwini Shinde: Formal analysis; Sarin Vijay Mythry: Investigation; Sarin Vijay Mythry: Methodology; Sarin Vijay Mythry: Project administration; Sarin Vijay Mythry: Resources; FB Shiddanagouda: Software; FA: Supervision; Sarin Vijay Mythry, FB Shiddanagouda: Validation; Sarin Vijay Mythry, FB Shiddanagouda: Visualization; Sarin Vijay Mythry, Jillela Venkateswar Rao: Roles/Writing – original draft; Sarin Vijay Mythry, N Dinesh Kumar, Shashi Kant Gupta, Sai K Oruganti : Writing – review & editing.

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