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Research Paper

Artificial Intelligence for VLSI Reliability: A Comprehensive Review of Machine Learning, Deep Learning, and Explainable AI for Fault Prediction and Diagnosis

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Abstract

The current trend of VLSI technologies focus on increasing chip complexity and efficiency by minimizing the size of the transistors which led to complexity in predicting and preventing faults in IC Fabrication. Traditional methods of fault detection are slow that cannot cope up with advanced Complex chip designs. Due to the advancements of the driving technologies machine learning (ML) algorithms have exponentially increased to foretell faults in VLSI circuits more precisely and effectively. This study explores different machine learning (ML) algorithms, categorizing them into supervised, unsupervised, and deep learning, and also discusses hybrid models to identify some common faults in VLSI circuits including stuck-at faults, bridging faults, open circuits and delay faults. Also the work focuses on the ways the data are gathered, that are significant in the process of training models and their evaluation performance. The paper discusses the on-going challenges in fault prediction and highlights how emerging techniques such as explainable AI can help address these complexities more effectively. This paper is a review-based study that aims to review and compare previous research on VLSI predicting faults and diagnosis using ML, DL and XAI techniques, without any independent simulation or experimental validation.

A total of 23 research papers published from 2020 to 2025 underwent through evaluation to gauge the utility of machine learning (ML), Deep Learning (DL) and hybrid models for VLSI fault prediction. The investigations are appraised using performance metrics, accuracy, precision, recall and F1 score. The review dissects diverse fault prediction paradigms, pre-processing techniques, feature extraction approach and learning infrastructure to diagnose faults in VLSI circuits. Future fault diagnosis systems using XAI, hybrid models are also discussed for future research needs in VLSI testing.

Keyword: VLSI testing, Fault prediction, LSTM, Support Vector Machine, Machine learning, Hybrid model, deep Learning, SSAE, Deep SAE, Explainable AI.

Introduction

With continuous transistor shrinking into Nano scale technologies, VLSI circuits have become highly complex. According to semiconductor industry reports, transistor density has increased from millions in early 2000 designs to tens of billions in modern processors, while feature sizes have reduced from 180nm to below 5nm nodes. As transistor dimensions shrink below 10nm, variability effects such as leakage current fluctuation, process variation, and timing uncertainty increase significantly. These nonlinear behaviours are difficult to model analytically, making data-driven machine learning approaches more suitable for fault prediction. This exponential growth significantly increases defect probability, parametric variability, and testing complexity, thereby motivating the adoption of machine learning-driven prediction methods.

This increases the dis-ingenuity of detection and prediction of faults before and after fabrication [1]. The traditional method of detecting faults contributes to human error and consumption of more time that leads to wrong fault detection. Fault prediction is important when there is a need to decrease testing of VLSI to optimize the test cycles. VLSI faults can broadly be categorized into fabrication-level faults and circuit-level faults. Fabrication faults originate during semiconductor manufacturing processes such as lithography defects, oxide breakdown, and particle contamination. Circuit-level faults occur due to design logic errors, timing violations, signal integrity problems, or aging effects during operation. Distinguishing these categories is important because fabrication faults require yield-aware prediction models while circuit-level faults demand behavioral and timing-aware learning methods

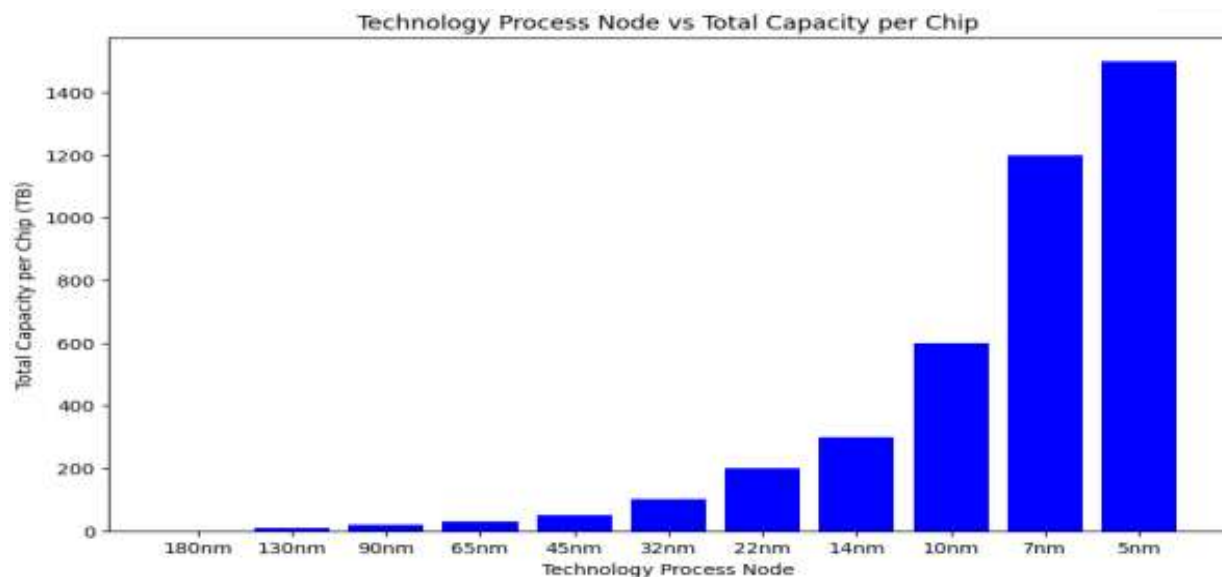


Fig.1 DATA CAPACITY VS CHIP TECHNOLOGY

Traditional methods depend on deterministic methods such as built-in self-test (BIST) techniques, design-for-testability (DFT) techniques, and fault simulation. These methods identify faults through predefined test patterns and exhaustive testing procedures. These traditional methods often fail to address the faults of modern VLSI circuits. The large number of test vectors required for exhaustive testing leads to long test times and high power consumption, which is not practical for advanced designs.

Over the past few years, Machine learning techniques are recognized as a powerful means of improving fault prediction in VLSI testing [2]. Numerous studies investigate the efficiency of Machine Learning (ML) and Deep learning (DL) based fault forecasting techniques in VLSI circuits. Khalil et al. [11] introduced a predictive system incorporating Fast Fourier Transform (FFT), Principal component analysis (PCA), Convolutional neural network (CNN) to attain high fault categorization precision. Lithana et al. [18] evaluated various machine learning (ML) models such as Convolutional Neural Network (CNNs), Support Vector machine (SVM), Random Forest (RF) and ensemble configurations reported substantial progress in defect tracking capabilities. Gaber and Hussein [19,22] implemented deep learning architecture like deep sparse auto encoder(DSAE) alongside stacked sparse auto encoder(SSAE) to tackle the difficulties in discovering stuck-at errors in digital circuits.

AI-driven diagnostic architectures have been investigated by the researcher to optimize error isolation and source analysis in VLSI systems. Ojha [20] established that combining machine learning procedures with neural network topologies boost the fault diagnostic capability. In a comparable approach, Lu et al. [21] utilized machine learning paradigms alongside graph neural network (GNN) to anticipate the outcomes from simulated fault injections thereby attaining prediction speed, scalability than convolutional simulation methods. In Moness et al. [23] introduced automated design anomaly debugging protocols utilizing deep learning, achieving excellent fault detection accuracy with minimal computational overhead.

This literature review delivers a structured review of Machine Learning (ML), Deep Learning (DL) and hybrid model for forecasting failures in VLSI Circuits and evaluation made based on fault coverage, accuracy, precision, Sensitivity and Computational overhead. It also fills existing research gaps and explores forward looking trends like explainable Artificial Intelligence (XAI), hybrid learning frameworks and smart diagnostic platforms for next generation semiconductor devices.

2. Research Methodology, Research Gap, and Contributions

This review uses a systematic literature survey to look at recent advances in applying machine learning (ML), deep learning (DL), and hybrid learning algorithms to predict and detect faults in VLSI circuits. We selected research papers published between 2020 and 2025 through an extensive search in key scientific databases, including IEEE Explore, Science Direct, Springer Link, Wiley Online Library, and Google Scholar. The keywords used in this search to ensure we included all relevant articles were VLSI Fault Prediction, Machine Learning for VLSI Testing, Deep Learning Fault Detection, Stuck-at Fault Detection, VLSI Reliability, Fault Diagnosis in Integrated Circuits, and AI-Based VLSI Testing. We chose papers by assessing fault prediction techniques, preprocessing and feature extraction methods, ML and DL models used, fault coverage, and performance measures such as accuracy, precision, recall, and F1-score. Despite significant improvements in using ML and DL algorithms for VLSI circuit fault detection, current literature reviews tend to focus only on conventional fault detection methods or specific learning algorithms without offering comparisons. Other emerging areas like explainable artificial intelligence (XAI) techniques, hybrid learning algorithms, automation in fault diagnostics, and intelligent reliability prediction also deserve attention.

3. Conventional Methods and Their Limitations in VLSI testing:

3.1 Design-for-Testability (DFT)

Circuits are designed using DFT techniques to facilitate testing. It includes the placement of more hardware like built-in self-tests (BIST), scan chains, and other easier to detect fault providing structures. DFT techniques often require additional circuit, which adds to the area and the power consumption of the chip and may cancel out the benefits of tailored designs. DFT may facilitate test, yet the more complex designs become the harder and time-consuming it may prove to integrate DFT structures into the design. DFT simplifies testing, integrating DFT structures can become complex and time consuming in intricate designs. The test vectors are used on a VLSI circuit in order to simulate faults. The testers can determine how signals ought to travel.

3.2 Built-In Self-Test (BIST)

This method integrates self-testing circuits into the VLSI design for automatic fault detection during fabrication while it simplifies testing and it might increase chip area and power consumption and might not detect all fault types. BIST might not be able to detect all types of fault, particularly those involving unusual or complicated failure modes.

3.3 Exhaustive Testing

This method guarantees fault-free operation, by running a VLSI circuit through every possible. This ensures that all potential errors are tested against the every possible set of inputs. Modern circuits cannot be tested sufficiently- the number of possible combinations of input to the circuit grows exponentially with the complexity of a VLSI design. Testing all possible vectors is highly costly and time-consuming especially with respect to complex systems. Due to this fact, production-oriented real life applications that have stringent production schedules are unable to carry lengthy testing. The huge power requirement in generating one test vector to operate is not good to low-power designs, especially in portable and battery controlled devices.

4. Machine Learning Roles in Fault Detection:

The increased precision in machine learning predictions should be listed among the main drawbacks of traditionally used methods. ML effectively adapts to the increasing complexity of VLSI circuits, which conventional methods struggle to manage. Traditional fault detection approaches face major bottlenecks including exponential test vector growth, inability to model process variability, lack of adaptive learning, and poor scalability for Nanoscale technologies. These constraints increase production cost and reduce test throughput in industrial test environments.

Machine learning models can be trained to recognize the fault patterns and predicts potential failures, allowing proactive issue resolution and fault location within the circuit. ML is a versatile technique for next generation designs, including 5G communications, AI chips and Internet of Things devices. This approach leads to reduced turnaround times, minimized defects and increased power efficiency in testing.

Self-learning functions of fault predictions can offer more power efficiency in testing as well as rising the precision and reducing time that can be spent on the example. Machine learning (ML) extends beyond mere fault prediction in circuits to encompass fault localization and diagnosis, significantly optimizing the debugging process. Algorithms such as classification algorithms and decision trees are instrumental in this application. ML algorithms can analyze sensor data, historical performance, and circuit diagrams to identify the specific component or area within a circuit most likely to be experiencing a fault. This is achieved by learning patterns associated with different fault types and their origins. Beyond pinpointing the location, ML can also infer the probable causes of the fault. For example, a decision tree might analyze voltage fluctuations, temperature readings, and current anomalies to suggest whether a fault is due to a short circuit, an open circuit, component degradation, or external factors like power surges. For instance, Support Vector Machines are effective in classification-based fault prediction, Random Forest improves robustness under noisy datasets, and Auto encoders help in anomaly detection, while LSTM networks capture temporal degradation patterns in reliability monitoring scenarios.

5. Data preprocessing or featurization:

Data pre-processing and feature extraction are crucial steps in machine learning-based VLSI fault prediction systems. The raw test data collected from circuits often contains noise, extra information, missing values, and irrelevant features that can negatively affect model performance. Therefore, pre-processing methods are used to improve data quality and increase the predictive ability of machine learning models.

5.1 FFT-Based Feature Extraction

The Fast Fourier Transform (FFT) is often used to convert time-domain signals into frequency-domain representations. In VLSI fault prediction, FFT helps identify frequency traits associated with circuit faults that might not be visible in the original signal. Different fault conditions usually produce unique frequency signatures, making it easier to classify and diagnose faults accurately. FFT-based feature extraction is especially useful for analyzing analog and mixed-signal circuits.

5.2 Principal Component Analysis (PCA)

Principal Component Analysis (PCA) is a method for reducing dimensionality. It transforms high-dimensional data into a smaller set of principal components while keeping most of the data variation. PCA removes redundant and

related features, lowers computational complexity, and improves model training efficiency. Many studies have shown better fault classification accuracy when PCA is combined with machine learning and deep learning models.

5.3. Z-Score Normalization

Z-score normalization standardizes feature values by adjusting them so they have a mean of zero and a standard deviation of one. This method ensures that features with large numerical ranges do not dominate the learning process. Z-score normalization is particularly helpful for algorithms like Support Vector Machines (SVMs), Artificial Neural Networks (ANNs), and clustering techniques.

5.4. Min-Max Scaling

Min-Max scaling changes feature values to a fixed range, typically between 0 and 1. This normalization technique improves the speed of convergence during model training.

SUPERVISED LEARNING:

The most widely adopted machine learning approach for VLSI circuit fault prediction is supervised learning. [4][5]. the technique makes use of labeled data to train a model, in which the input features correspond to predetermined outcomes. The model can then be used to predict faults in new, unseen designs by learning the relationship between design features and fault occurrence. The support vector machines and neural networks, for example, can reveal hidden connections between circuit properties and fault events, enabling more precise fault prediction and detection. [7][8]. There are two main types of algorithm that exists in supervised learning. one is classification and another one is regression algorithm. The classification algorithm classifies the output to two target classes. The two categories in which classification is divided are binary classification and multiclass classification. Whereas the continuous numerical values are predicted with the help of the regression algorithm. Examples of regression models include linear regression (LR), polynomial regression (PR), decision trees (DT), random forest (RF), K-Nearest Neighbors (KNN) which helps in making predictions easier. Under limited training data conditions, SVM, Random Forest, and Gradient Boosting models often outperform deep neural networks due to lower data dependency.

A supervised learner constructs a model using training data that will accurately predict new, unseen data of the same nature as the training data used to construct the model. The capacity of a model to produce correct predictions on previously unobserved data can be called its capacity to generalize based on the training examples to the test examples.. The point is to construct a model that generalizes as closely as possible. Over-fitting is the construction of a model that is more complex than the amount of information present. Fitting a model to the details of the training set, such that the model fits to the training set, but does not generalize to new data, is referred as over-fitting. When one selects a model that is too simple, it is said to be under fitting and therefore predicts incorrect values. Limited fault datasets often cause over fitting in deep learning models. Regularization, dropout, and cross-validation strategies are necessary to ensure generalization.

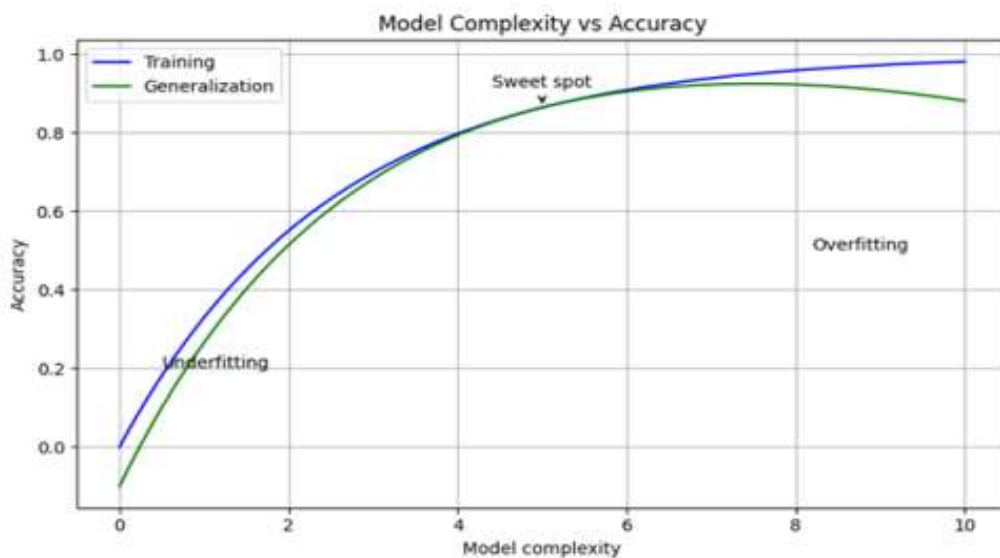


Fig.2 Model complexity Vs Accuracy graph

6.1 Mathematical Models of Machine Learning Algorithms

The basics of math that machine learning algorithms are built on help us understand how models that predict faults learn from test data for Very Large Scale Integration systems. The following equations show the basic math that Support Vector Machines, Random Forest, Artificial Neural Networks and Clustering algorithms use to work. Machine learning algorithms like Support Vector Machines and Artificial Neural Networks learn from test data to make predictions. The math behind machine learning algorithms is important for understanding how models like Random Forest and Clustering algorithms work with test data, for Very Large Scale Integration systems.

6.1.1 Support Vector Machine (SVM)

Decision Function: $f(x) = w^T x + b$

Optimization: minimize $(1/2)||w||^2$

Subject to: $y_i(w^T x_i + b) \geq 1$

6.1.2 Random Forest (RF)

Prediction: $\hat{y} = \text{mode}\{T_1(x), T_2(x), \dots, T_n(x)\}$

Gini Index: $\text{Gini} = 1 - \sum (p_i^2)$

6.1.3 Artificial Neural Network (ANN)

Neuron Model: $z = \sum (w_i x_i) + b$

Activation Function: $f(z) = 1/(1 + e^{-z})$

Weight Update: $w_{\text{new}} = w_{\text{old}} - \eta(\partial E / \partial w)$

6.1.4 Clustering (K-Means)

Distance Measure: $d(x_i, c_j) = \sqrt{\sum (x_{ik} - c_{jk})^2}$

Objective Function: $J = \sum \sum ||x_i - c_j||^2$

Unsupervised learning:

When labeled data is difficult to get by or unavailable, unsupervised learning techniques are employed. Without explicit supervision, these algorithms are capable of to detect patterns or anomalies in the data (i.e., without knowing whether the circuit is faulty or not). By determining odd patterns in test results or design parameters, unsupervised techniques like anomaly detection and clustering are frequently employed to predict faults [8]. A common application of dimensionality reduction unsupervised transformations Transforms: Transforms represent a high-dimensional representation of the data, or a large number of features, in a new representation that reflects the important properties with fewer features. Two-dimensional reduction is another common application of dimensionality reduction to visualization. Rather, clustering algorithms categorize the data into various clusters of similar items.

Deep learning

Deep learning is among the latest and most effective methods of automatic feature extraction and fault detection. Fault detection performance is better in comparison with the traditional method because of the utilization of significant data and the aim to find the most valuable characteristics with the help of deep learning. ANNs perform such tasks as the diagnosis of faults and complex classifications due to fitting the complex functions using the nonlinear transformation. Some of the common ANN types used include:

Feeding forward neural networks (FNNs) work one way with the input data. Recurrent neural networks (RNNs) come in handy in such tasks such as text-to-speech conversion since they have memorized cells to predict outputs. Computer vision and image processing are excellently suited to the convolution neural network (CNN) framework since the model computes input properties by batches.[9]Modular neural networks (MNNs) which comprise of distinct networks that handle sub problems are beneficial in applications like modelling, character recognition and so forth.

8.1 Deep Learning Approaches for VLSI Fault Prediction

Deep learning has become an important method for predicting and diagnosing faults in VLSI circuits because it can automatically spot complex patterns in large datasets. Unlike traditional machine learning methods that rely on a lot of manual feature work, deep learning models can extract features in layers, which improve prediction accuracy. The most commonly used architectures are Feed forward Neural Networks (FNNs), Recurrent Neural Networks (RNNs), and Convolutional Neural Networks (CNNs).

8.1.1 Feed forward Neural Network (FNN)

A Feed forward Neural Network (FNN) is the simplest type of artificial neural network. In this design, information flows in one direction, from the input layer to the output layer, passing through one or more hidden layers. There are no feedback connections or cycles in this network. Every neuron in one layer connects to every neuron in the next layer, creating a fully connected setup.

An FNN works through forward propagation. In this process, input features multiply by weights, combine with bias values, and pass through nonlinear activation functions to produce outputs. During training, the network adjusts its weights using optimization methods like Gradient Descent and Back propagation to lower prediction errors.

In VLSI fault prediction, FNNs are widely used for static fault classification. Here, fault patterns are represented by fixed input features from test data. Their ability to model nonlinear relationships between circuit parameters and fault conditions makes them effective at identifying manufacturing defects, stuck-at faults, and reliability issues. However, FNNs may struggle to capture temporal dependencies in sequential fault data.

8.1.2 Recurrent Neural Network (RNN)

A Recurrent Neural Network (RNN) is a specific type of neural network designed for handling sequential and time-dependent data. Unlike FNNs, RNNs have feedback connections that help them remember previous inputs. This feature makes RNNs well-suited for tasks where context and order are important.

8.1.3 Convolutional Neural Network (CNN)

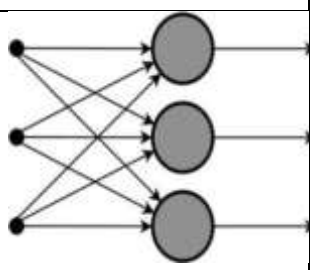
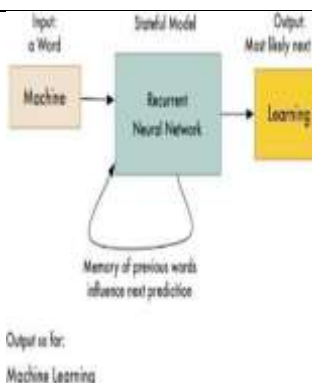
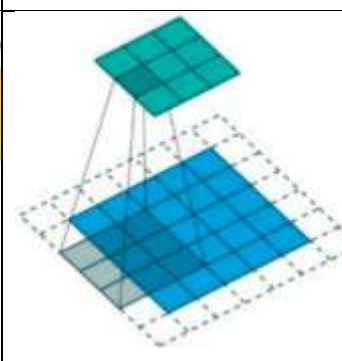
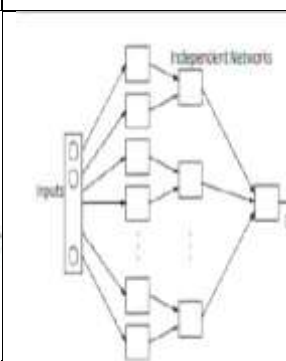
Convolutional Neural Networks (CNNs) are deep learning frameworks designed for feature extraction and pattern recognition. These networks consist of several layers, including convolution layers, pooling layers, activation layers, and fully connected layers.

The convolution layer uses learnable filters on the input data, enabling the network to identify local patterns and traits linked to faults. With each convolution operation, the model learns gradually more complex representations of features. After convolution, pooling layers reduce the size of feature maps while keeping important information, which lowers computational load and reduces the chance of over fitting.

A key advantage of CNNs is their ability to automatically extract features. This removes the need for extensive manual preprocessing. For VLSI fault prediction, CNNs can extract relevant features from circuit layouts, wafer maps, fault images, scan-chain outputs, and testing datasets. This capability helps accurately identify fault signatures and improves classification performance compared to traditional machine learning methods.

Recent research shows that CNN-based models achieve high accuracy in fault detection because they effectively capture spatial relationships and hidden fault characteristics within complex circuit data. As a result, CNNs have become one of the most commonly used deep learning methods for intelligent VLSI fault diagnosis and prediction. In summary, FNNs, RNNs, and CNNs provide different functions for VLSI fault prediction. FNNs are good for static classification tasks, RNNs are suitable for monitoring faults over time and forecasting reliability, while CNNs shine in automatic feature extraction and recognizing fault patterns. The choice of the best architecture depends on the nature of the fault data, computational requirements, and prediction goals.

TABLE I COMPARISON OF FNN, RNN, CNN, MNN

FNN	RNN	CNN	MNN
process input data in a single direction	useful for tasks like text-to-speech conversion	Useful for computer vision and image processing.	Useful for function approximation and character recognition.
			

Literature of fault prediction using ml and dl

The Study focuses on detecting stuck-at faults in digital VLSI. Two stuck-at faults exist. One is stuck-at 0 and one is stuck-at 1. A single stuck-at fault in a single line can cause lots of faults. Many situations or problems are tested with the help of the test vectors. The faults are identified through different test pattern generation in the conventional way. This is excessive of time-consuming and proves to be more complicated when the circuit is complex. [10]. To deal with that, ML-based algorithms may be employed in fault detection. The ML fault detection algorithm mainly used supervised model to predict huge amount of faults as it learns from the historical data. ML models predict the faults by prediction-based techniques like supervised learning (i.e.) classification & regression. Classification-based models aim to predict the fault by two categories (i.e.) YES / NO, While the regression algorithm detects/predicts faults by using new data points. Fault feature extraction plays a vital role in fault diagnosis process like wavelet transform, decision trees and support vector machines, ANN, etc.

These techniques lack effective non-linear fitting ability. The parameters depend on the past experience, and are unable to predict complicated faults. Ultimately, the performance is affected. This can be overcome by combining different models of ML and deep learning algorithms. Feature extraction plays a vital role in fault diagnosis. Techniques like wavelet transforms, decision trees, and support vector machines (SVM), artificial neural networks (ANN), etc., are used due to their effective nonlinear fitting ability. These techniques majorly depends upon the

input parameters derived from real time experiments .these techniques not able to predict the intricate fault and requires enhancement in performance. This drawback can be overcome by improving feature extraction and processing techniques.

In [11] presents a learning-based approach for hardware fault prediction which utilizes FFT (Fast Fourier Transform) and PCA (Principal Component Analysis) focusing on frequency-based signal signatures. The proposed method integrates PCA and CNN (Convolutional Neural Network) demonstrates high accuracy 98–99% accuracy across various circuits. FFT is used to analyze signals in the frequency domain, where Low to high frequency components indicate the early fault prediction. Frequency with different bands represents varying faults and their different bands. The second stage, PCA, eliminates the unwanted data. Streamlining the analysis process. PCA's output is used for fault classification. CNN receives the PCA's output result to produce the output result. SVMs do not contain much information to get correct result. This technique provides sufficient data by using FFT; by providing character of fault, input from FFT in frequency domain is used. This paper presents a technique of FFT (Fast Fourier Transform) and PCA (Principal Component Analysis) for fault prediction of circuits. This technique is tested in comparator and amplifier circuits.

Hybrid model Vs Standalone model:

A promising way to deal with issues is artificial intelligence (AI). Artificial intelligence (AI)-driven fault detection systems use neural networks and machine learning algorithms that autonomously locate, classify, and identify issues with VLSI circuits.

Such systems are more helpful in real-time diagnostics because their algorithms may learn all the previously experienced faults and detecting subtle error tendencies overlooked by traditional methods. The methodology aims to reduce fault coverage, reduce test time and facilitate root-cause analysis to faster repair and optimized in VLSI circuits. Previous studies have demonstrated through simulations and comparative analysis that AI-based approaches outperform conventional fault detection methods.

With a move toward developing new chip designs to be smarter and diagnosing themselves, this study opens the way to developing stronger and better performing electronic systems. SVMs are used for locating intermittent faults in high-speed circuits, while clustering methods like k-means are explored for unsupervised fault identification, although they face challenges with high-dimensional data in modern VLSI designs. CNN-based methods are shown to outperform conventional techniques in accurately identifying small layout problems.

Deep learning faces challenges in VLSI fault detection due to the difficulty in obtaining large datasets and the need for substantial computational resources. Deep learning models are often not easily interpretable; making root-cause analysis difficult in VLSI fault detection. AI integration into VLSI fault detection can effectively address issues in modern electronics. Hybrid models combining machine learning algorithms and rule-based systems enhance problem recognition and diagnosis in this field. To illustrate, hybrid systems that integrate ML models and genetic algorithms are used to optimize test patterns to increase fault coverage with a reduction in test time. Furthermore, recent advances involve reinforcement learning (RL) for dynamic fault

In [13] uses a hybrid model of LSTM-SVM model to predict machine failure. The motivation behind combining LSTM and SVM lies in their complementary strengths. LSTM captures temporal dependencies and sequential degradation patterns, whereas SVM provides strong decision boundaries for classification. The hybrid model leverages temporal feature extraction from LSTM and robust classification from SVM, improving prediction stability and accuracy. This can be tested by using three public datasets .validation set is also introduced to upgrade the system performance. The architecture consists of four layers: input layer, hidden layer and (FC) fully connected layer, softmax layer. 60%data is of training set, 20%validation set, 20% testing set. LSTM network is enhanced by SVM classifier for better results.

The comparison table is produced below.

Table II: Comparison of SVM, LSTM, LSTM-SVM

DATA	Author	Model	Accuracy (%)	Precision (%)	F1-Score (%)	Recall (%)
DATA I	OuiamKhattach Omar Moussaoui Mohammed Hassine	SVM	95.86	79.20	80.08	80.98
		LSTM	97.01	82.36	88.85	96.46
		LSTM-SVM	97.72	97.70	97.71	97.72
DATA II		SVM	86.54	100	78.23	64.25
		LSTM	94.58	94.79	94.63	94.58
		LSTM-SVM	97.17	96.32	96.86	97.47
DATA III		SVM	92.51	96.41	87.91	80.71
		LSTM	97.51	96.95	96.31	95.61

		LSTM-SVM	98.15	97.43	97.91	98.51
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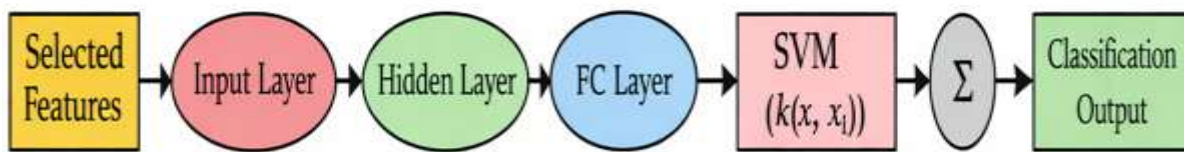


Fig: 3 Hybrid architecture of LSTM-SVM

The evaluation metrics is calculated using the formula:

$$Accuracy = TP + TN / TP + TN + FP + FN \quad (1)$$

$$Precision = TP / TP + FP \quad (2)$$

$$Recall = TP / TP + FN \quad (3)$$

$$F1\text{-score} = 2 * Precision * Recall / Precision + Recall$$

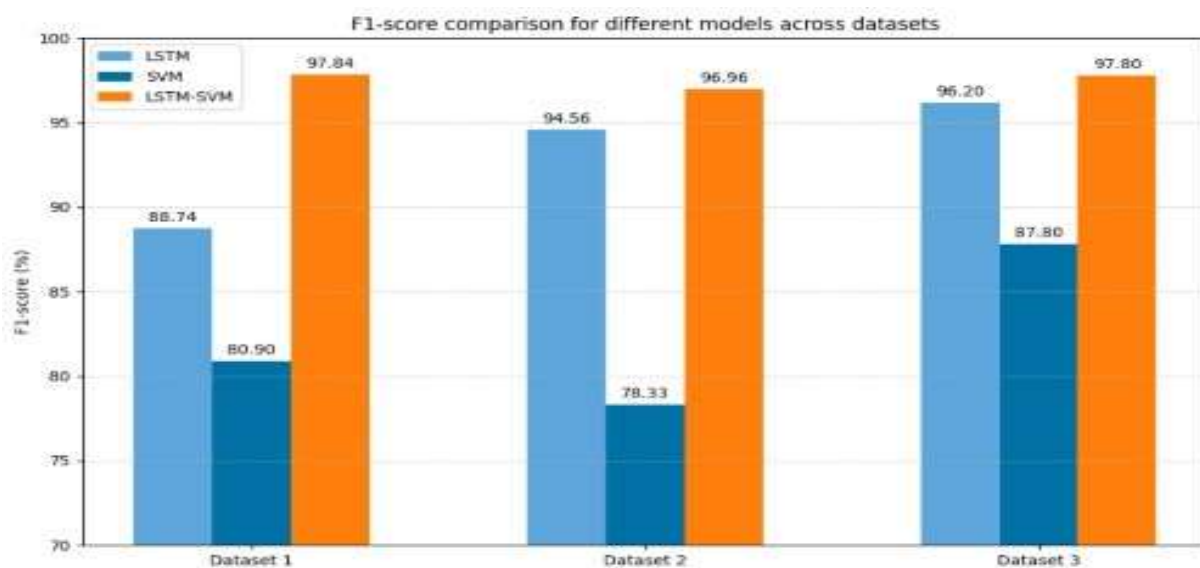


Fig: 4 Performance of the three models on the three datasets

From the above figure, LSTM-SVM hybrid model produces more accurate results of 97% compared to standalone models of LSTM and SVM. The hybrid approach is a promising avenue to improving classification, especially when one considers a failure prediction task. In the referenced study, the batch size was experimentally tuned to improve model convergence; however, in practical implementations, batch sizes such as 32 or 64 are typically preferred for stable gradient convergence. The reliability and accuracy of failure prediction models in a number of areas including fault detection and predictive maintenance can be enhanced by employing machine learning methods to find unusual patterns in data [14]. An overview of failure methods for forecasting based on deep learning and machine learning is provided in this survey. Time series forecasting is still a very crucial area in predictive analysis since there exists various models which have been successfully established on various areas. However, there is a grave issue of selecting the most appropriate model to a given application as time-dependent data is dynamic and multilateral in character. In [15] recent years, a keen interest fell towards hybrid modeling mechanisms, i.e. the combination of multiple machine learning (ML) and deep learning (DL) approaches. The concept of these hybrid structures is to combine the merits of the different algorithms to enhance their predictive skills and consistency e.g. Explainability of the regular ML algorithms versus the representation learning capacity of DL architectures to have higher general forecasting performance robustness.

In [16] New hybrid architecture with Convolutional Neural Networks (CNN) associated with Long Short-Term (LSTM) networks has been introduced regarding predictive maintenance. Here, the CNN module is able to self-learn complex temporal characteristics of raw time series and the LSTM cell models sequence dependence to make precise predictions. This combination of CNNs and LSTM can reliably surpass other methods, including CNN or LSTM, because of the combined strengths that they have on spatial features extraction and long-term temporal dynamics. The results show that hybrid framework provides better prediction accuracy and is an effective and reliable method of predicting in predictive maintenance, especially in the early detection of failures and high system reliability.

In [17] proposed a model which combines LSTM for time series pattern modeling and CNN for efficient feature extraction from variable time series data, enabling streamlined maintenance programs and improved performance of electric machines. A hybrid network was introduced to accurately predict delayed maintenance in wind turbines, optimizing power utility operations management. This architecture synergistically combines CNNs for effective feature extraction and SVMs for establishing robust decision limits, particularly using CNN-extracted features to train Radial Basis Function (RBF) SVM classifiers. The combination of deep learning for feature extraction and advanced classification techniques demonstrates the success of these hybrid approaches in developing predictive maintenance strategies for the energy industry.

In [18] proposed, and then automated AI&ML system for fault detection. They employed various ml algorithms like CNN, SVM and Random forest to classify and detect faults in various circuits. The authors also proposed various hybrid algorithms for fault detection that provides maximum fault. Coverage, the results as being tested in ISCAS' 85.Benchmark test data sets. The experimental results of CNN ITC-99 provide 95.8%, accuracy, 93.1%, accuracy in SVM 94.3%, RF and 97.6% in ensemble methods. The results suggest that CNN suits. Well, for stuck at, bridging Faults at 97.2 % and 96.4%. From the comparative table it is observed that ensemble methods achieves high accuracy, Precision, Recall and f1 score of about 97.6%, 96.8%,97.9%, 97.3%.

Deep Learning frameworks

Deep learning, particularly deep neural networks (DNNs), are utilized for VLSI fault prediction due to its capacity to acquire structural representations from raw data. DNNs, convolutional neural networks (CNNs), and recurrent neural networks (RNNs) are utilized for VLSI fault prediction, especially for complex circuits where traditional models fall short. In [19] focus on stuck-at fault detection model developed on techniques for deep learning. The main challenge in traditional algorithms is an exponential growth of the search space with increase IC complexity. The study proposes developing two separate models: a semi-supervised model and a supervised model to reduce the dimensionality of characteristics represent IC design with the supervised model relying on Multi-Fidelity Optimization; the previous one is based on Deep Sparse Auto-encoder. The maximum validation accuracy of our initial model is almost 98%. By using a Multi-Fidelity method as an optimization tool to find the best solution, the second proposed model seeks to detect stuck-at defects in digital circuits without requiring for a feature extraction process.

In [20] proposed AI- augmented method for fault detection, and diagnosis in VLSI circuits. The author combines ML algorithm with NN to improve the fault detection method in VLSI circuits. The simulation based approach results in time consuming. So AI based methods SVM XG Boost are employed to detect fault easier and root cause of the fault has been sort out.ML algorithms like RF, SVM, XGBoost for fault detection and neural networks like multilayer perceptron (MLP) is used to predict the fault in the circuit. The experiment results produces fault Detection, accuracy of 98.5% in RF and SVM 96.8% and in XGBoost 97.4% neural network, locate the fault in 94.2% due to hidden nature of deep learning algorithms. It is difficult to locate the exact path or node of fault.

In [21,22] proposed machine learning based fault prediction from the results in simulation based injection of faults. The proposed method using neural networks and GNN to predict faults in six different circuits thereby, increasing the speed of fault prediction in circuits. The experimental results prove that GNN's performance is comparatively better than NN's. Basically, two types of faults S-A-0 and S-A-1 has been tested on XGE- MAC and ETH-MAC circuits and comparative table has been given between normal simulation time of NN, GNN. GNN takes simulation less than 0.5 hours compared for NN.

In [23, 24] proposed a deep learning space called SSAE for fault detection and correction in VLSI circuits. This method overcomes the search space explosion problem in SAT Solvers. The test pattern has been generated by Atalanta software and is implemented on 8 Combinational circuits on ISCAS'85. The experimental results through that Atalanta tool delivers 99.2% of fault coverage, SSAE delivers 99.7% accuracy in fault reduction.

In [25] proposed a method for automatic fault detection, in Complex VLSI circuits. They used methods like stacked sparse auto encoder for stuck at fault detection, in both combination and sequential circuits. This method resolves the computational time complexity in, sat solvers. Automatic test pattern, generation tools, like Atlanta has been employed which overcomes the limitations of Max- Sat approach. This process achieves fault. Accuracy around a 99.6% in combinational circuits from ISCAS' 85 and 99.8% In sequential circuits from is ISCAS' 89 Benchmark Circuits. Various auto encoder types, [26] like a deep sparse AE,AE, stacked sparse AE has been compared to find the best model for feature extraction and concluded 99.95 % deep sparse AE Works good for combinational circuits and stacked sparse AE is good for sequential circuits. However, this method suffers from more data set collection to approximate connection between lines perfectly to detect the main reason for faults. The Future work focuses on developing Explainable AI model for fault detection and to combine the system with an edge device to increase real-time, performance.

Table III. Comparison table for Machine learning and Deep learning Algorithms

Authors	Model	Accuracy (%)	Precision(%)	F1-Score(%)	Recall(%)
Ouiam Khattach,	SVM	95.86	79.20	80.08	80.98
	LSTM	97.01	82.36	88.85	96.46

Omar Moussaoui, Mohammed Hassine[12].	LSTM-SVM	97.72	97.70	97.71	97.72
	SVM	86.54	100	78.23	64.25
	LSTM	94.58	94.79	94.63	94.58
	LSTM-SVM	97.17	96.32	96.86	97.47
	SVM	92.51	96.41	87.91	80.71
	LSTM	97.51	96.95	96.31	95.61
	LSTM-SVM	98.15	97.43	97.91	98.51
Lithana,M,A, Loshna, k, Prabu, Arulraj[18].	CNN	95.8	94.6	95.4	96.3
	SVM	93.1	92.4	93.1	93.9
	Random Forest	94.3	92.8	94.2	95.6
	Ensemble	97.6	96.8	97.3	97.9
Moness,M, Gaber,L, Hussein[23].	VAE	99.6	-	-	-
	SSAE	99.8	-	-	-
	Deep SAE	99.95	-	-	-

In table [III] Comparison of machine learning and deep learning algorithms like SVM, LSTM LSTM- SVM (hybrid model), Random forest, Ensemble, VAE, SSAE, Deep SAE based on their accuracy, precision, recall, F1 score, metrics performance results has being tabulated.

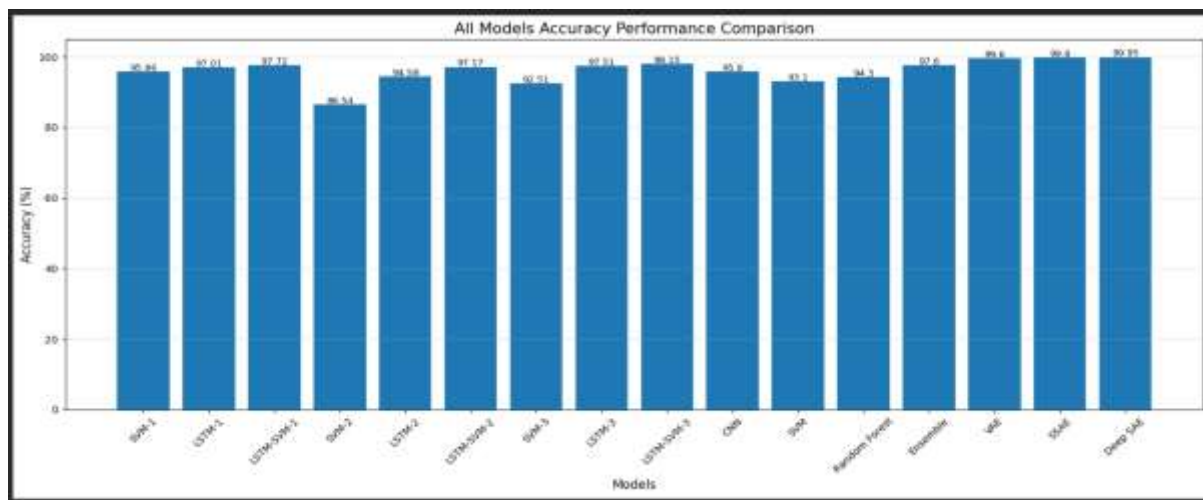


Fig 5. ML & DL Models Accuracy Performance Metrics

Figure 5 represents comparison of Machine Learning and Deep Learning accuracy analysis performance metrics.

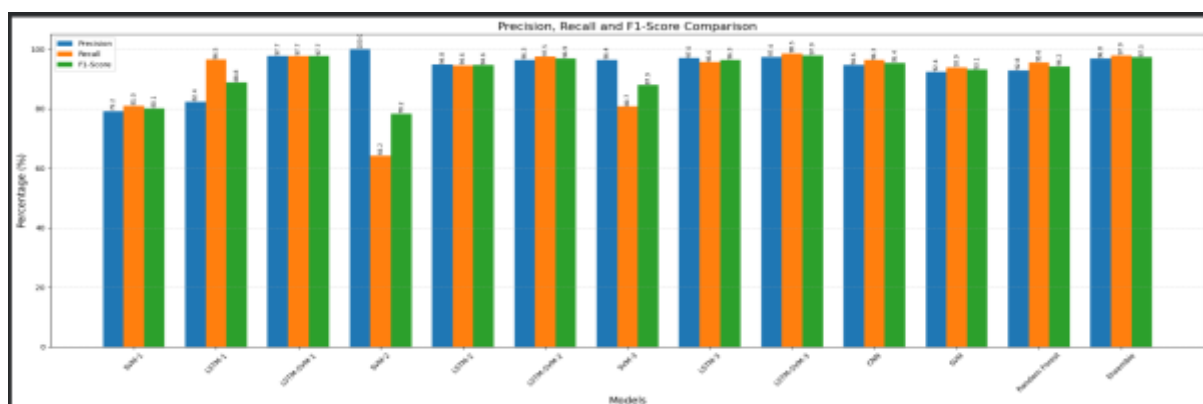


Fig 6. ML & DL Models Performance Metrics Graph

Figure 6 shows the graph representing accuracy. Precision, Recall, F1score metrics. The result shows that deep sparse auto encoder suits best for fault prediction in Complex VLSI circuits with accuracy of 99.95%.

The key contributions of this survey include a unified comparison of standalone and hybrid machine learning models and Deep Learning models for VLSI fault prediction, along with a systematic mapping of different fault types to the most suitable machine learning architectures. The study also identifies critical dataset limitations that

affect prediction performance in VLSI testing and highlights the emerging role of explainable AI techniques in improving transparency and reliability in chip diagnostics.

As a result, many authors resort to benchmarks and simulated test data which fail to truly represent the manufacturing environment. The collection of fault data from the manufactured integrated circuit chips is tedious and expensive and often restricted by Intellectual Property (IP) issues. Hence, many researchers solely rely upon benchmarks and simulated test data that do not reflect the manufacturing context in an accurate manner. Therefore, more emphasis should be placed on developing large scale public datasets and methods for synthesizing fault data to enhance model generalization.

Class Imbalance Issue:

Fault datasets generally consists of considerably lesser number of faulty samples compared to normal operating samples, which leads to machine learning models leaning towards the majority class and poor prediction capability. Hence, efforts must be directed towards advanced data balancing strategies like Synthetic Minority Oversampling Technique (SMOTE), cost sensitive learning, and adaptive sampling to correctly detect less frequent fault occurrences.

10.1 Interpretability of deep learning models:

Although deep learning models often yield highly accurate predictions, the decision-making process of deep learning models is often opaque, posing a challenge for deployment in safety critical applications of the semiconductor industry where it is essential for engineers to be able to comprehend the fault prediction reasoning. Techniques from Explainable AI (XAI) can provide insights to the black box decision making process of models using SHAP, LIME, attention mechanism and feature attribution methods.

10.2 Real-Time FPGA Implementation

At present, most fault prediction systems have been validated using software simulations or offline experiments. However, the application in real world needs to be implemented on hardware platforms, such as FPGAs, so as to predict faults at real-time. FPGA-based acceleration is a promising method that provides low-latency fault prediction and allows circuit health to be monitored on-chip. Future work can explore the development of light weight neural network architectures or hardware friendly AI models for real time implementation on FPGAs.

10.3 Computational Complexity

Complex deep learning architectures typically require large computation resources, memory, and training time. Implementation costs and the feasibility in resource constraint applications increase. Model compression techniques such as pruning, quantization, knowledge distillation, and hardware-aware optimization could be helpful for reducing the computation complexity and retaining high accuracy.

10.4 Scalability for Advanced Technology Nodes

With the rapid advance of semiconductor technology toward sub-5 nm and future nanoscale technology, the fault mechanisms become increasingly complex because of process variations, aging effects, leakage currents, manufacturing uncertainties, etc. It is challenging to adapt the current fault prediction models to the advanced technology nodes. The research toward scalable learning frameworks that are capable of dealing with the tremendous design complexity, heterogeneous structures, and next-generation semiconductor technologies is needed.

Conclusion

Even though many research shows that AI and ML algorithms are efficient in fault products VLSI recognition, a lack of literature can be seen on studies of AI and ML methods as a whole within the scope of forecasting the VLSI in fault. VLSI fault detection methods are not complete and have critical gaps that need to be addressed. Existing literature primarily focuses on local fault detection, indicating a need for broader research. The challenge is to research towards creating robust, scalable, and smart fault-detection systems to pave the way to greater dependable VLSI circuits. Future VLSI fault prediction systems are expected to integrate explainable AI, adaptive online learning, and cross-layer reliability monitoring to create intelligent self-diagnosing chips. Such systems will enable early fault detection, automated root-cause analysis, and predictive maintenance in next-generation semiconductor devices.

The future VLSI fault prediction systems are supposed to integrate machine learning, deep learning, explainable AI, edge intelligence, and hardware acceleration. Hybrid architectures which combine data-driven learning and domain knowledge are promising in achieving higher accuracy and reliability. Furthermore, adaptive online learning and self-healing circuit design techniques could enable the intelligent semiconductor devices to achieve real-time monitoring diagnose and perform proactive repair.

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