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High-Voltage Silicon Carbide Traction Inverter Development for Heavy-Duty Electric Trucks: Design, Simulation, and Experimental Validation

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Abstract
A detailed design, MATLAB/Simulink simulation and experimental validation of an 800 V/350 kW Silicon Carbide (SiC) MOSFET based heavy duty Class 8 electric trucks traction inverter are presented in this paper. The proposed 3-phase 2-level voltage source inverter (2L-VSI) uses 1200 V SiC MOSFET half-bridge modules and has a conversion efficiency of 98.46% at the rated load of 250 kW. A new integrated liquid-cooled busbar with a stray inductance of just 9.8 nH in the commutation loop lowers stray inductance in the busbar loop. A high-fidelity MATLAB/Simulink three-level model hierarchy is used to obtain simulation results for both steady state and transient conditions, which are compared with hardware measurements. Experimental results from a dynamometer test bench and vehicle-level testing, on a 44 tonne truck platform, verify that the current THD is sub-2%, junction temperatures are within 98°C at peak load, and compliance with ISO 26262 ASIL-C, CISPR 25 Class 3 and UN ECE R100 standards is confirmed.

Keyword: Electric trucks, traction inverter, silicon carbide MOSFET, MATLAB/Simulink, SVPWM, dead time compensation, thermal management, ISO 26262, heavy duty EV.

I. Introduction

The progress of BEV Class-6 to Class-8 trucks has been rapid, with major OEMs aiming for an all-electric platform, ranging from 40–44 tones, for commercial deployment by 2027. The key power electronics assembly in the system, the traction inverter, is the most critical power electronics assembly in the system for efficiency, system performance, thermal load, and functional safety. The 800 V DC bus architecture is the enabling semiconductor for next generation traction inverters with Silicon Carbide (SiC) MOSFETs. They combine low switching losses (usually a quarter of Si-IGBT at the same current ratings), high thermal conductivity (3 times Si), and junction temperature ratings of above 175°C, making them ideal for the high-power, high duty cycle requirements of commercial vehicles. To realize these benefits in an inverter designed for production, however, careful co-optimization of the power stage, thermal management system, gate driver and closed-loop control is required, all of which are non-trivial engineering challenges at the 800 V / 350 kW level.

Prior literature has extensively documented SiC traction inverters for passenger EVs [1]–[4], but comparatively limited work addresses the specific constraints of heavy-duty truck applications: power ratings of 200–400 kW, 10,000-hour operational life, sustained high-current operation at elevated coolant temperatures (up to 70°C), and ISO 26262 ASIL-C functional safety requirements for torque control. Main contributions in this paper are (i) a complete system design methodology; (ii) a high-fidelity MATLAB/Simulink switching model with simulation results across key operating scenarios; (iii) detailed simulation-to-hardware correlation; and (iv) vehicle-level validation on a 44-tonne test truck.

II. Related Work

The evolution of SiC traction inverter technology has been extensively documented. Biela et al. [1] provided an early comparative study of SiC versus Si at 100 kW, establishing the theoretical loss advantage of SiC with up to 50% reduction in switching losses. Wolfspeed's automotive qualification roadmap [2] established the reliability basis for production traction inverter designs, including gate oxide reliability and short-circuit withstand capability.

In high-power module design, Wang et al. [5] proposed double-sided cooling for 1200 V SiC half-bridge modules, demonstrating a 35% reduction in junction-to-coolant thermal resistance. Complementary work on low-inductance packaging by Josifovic et al. [6] demonstrated that planar busbar geometries with integrated capacitors could reduce commutation loop inductance to below 15 nH. Control-side advances include the adaptive dead-time compensation method of Leggate and Kerkman [12], extended by Kim et al. [13] for sub-1% THD improvement.
In terms of functional safety, Papadopoulos et al. [16] proposed a framework to decompose ISO 26262 applicable to the traction inverter sub-systems. These bases are extended to 350 kW Class-8 truck operation with full simulation-to-hardware correlation in the present work.

III. SYSTEM ARCHITECTURE AND POWER STAGE DESIGN

A. Overall System Architecture

The traction inverter system follows a three-phase two-level voltage source inverter (2L-VSI) topology. The 800 V nominal DC bus interfaces to the HV battery via a manual service disconnect (MSD) and pre-charge relay. The inverter output drives a 6-pole interior permanent magnet synchronous motor (IPMSM) rated at 250 kW continuous / 350 kW peak with a base speed of 2,500 rpm and maximum speed of 6,000 rpm. Table I summarises the key electrical specifications.

TABLE I Key Electrical Specifications of the Traction Inverter

Parameter	Value
DC Bus Voltage (nominal)	800 V
DC Bus Voltage (range)	600 V – 920 V
Peak Output Power (30 s)	350 kW
Continuous Output Power	250 kW
Peak Phase Current (RMS)	450 A
Switching Frequency	10 kHz (adjustable 8–16 kHz)
DC Link Capacitance	450 µF (film, 1000 V)
Peak Inverter Efficiency	98.46% @ 250 kW, 800 V
Power Density	40 kW/L
Coolant Inlet Temperature	65°C (max)
Operating Temperature (ambient)	−40°C to +55°C
Enclosure Rating	IP6K9K per ISO 20653
EMC Standard	CISPR 25 Class 3

B. Power Module Selection and DC Link Design

The power stage features six 1200 V / 400 A SiC MOSFET half-bridge modules, housed in Kelvin-source packages. The temperature coefficient of SiC is positive, meaning that $R_{DS(on)}$ increases with temperature, allowing for intrinsic current sharing in parallel configurations with each module having $R_{DS(on)}$ = 2.4 mΩ at 25°C, and reaching $R_{DS(on)}$ = 4.6 mΩ at 150°C. The DC link capacitor bank is composed of twelve capacitors with a total of 450µF of metallised polypropylene film (MPPF), 37.5µF each. Based on the 2% ripple specification, the required capacitance of the DC link is:

$$C_{DC} \geq I_{phase,pk} / (8 \cdot f_{sw} \cdot \Delta V_{DC}) = (450\sqrt{2}) / (8 \times 10000 \times 16) \approx 498\ \mu F \quad (1)$$

The selected 450 µF is sufficient because at maximum modulation index M = 0.9 and unity power factor, simulation (Section V) confirms actual ripple of 14.2 V p-p—within the 16 V specification.

C. Integrated Liquid-Cooled Busbar

The integrated liquid-cooled busbar (ILCB) simultaneously minimises commutation loop stray inductance and manages DC link capacitor thermal load. The ILCB achieves L_{stray} = 9.8 nH (measured at 1 MHz). The resulting maximum switching overvoltage at dI/dt = 3000 A/µs is:

$\Delta V = L_{stray} \cdot dI/dt = 9.8\times10^{-9} \times 3\times10^{9} = 29.4\ V$ (2)
This limits peak device V_{DS} to 829.4 V, providing a 370 V margin to the 1200 V device rating.

IV. THERMAL MANAGEMENT SYSTEM

A. Cauer Thermal Network Model

A four-element Cauer thermal network models the junction-to-coolant heat path. Total thermal resistance is:
$R_{th,j\text{-}coolant} = R_{th,j\text{-}case} + R_{th,TIM} + R_{th,coldplate} = 0.018 + 0.008 + 0.009 = 0.035\ K/W$ (3)
At 350 kW peak with 933 W dissipated per switch position, the junction temperature rise above 65°C coolant is:
$\Delta T_j = P_{loss} \cdot R_{th,j\text{-}coolant} = 933 \times 0.035 = 32.6\ K \rightarrow T_j = 97.6°C$ (4)
This is well within the 150°C continuous and 175°C absolute maximum ratings.

B. Cold Plate CFD Analysis

Pin-fin cold plate geometry (diameter 2.5 mm, height 8 mm, staggered 4 mm pitch) was optimised by ANSYS Fluent CFD. At 12 L/min of 50% EGW coolant, Re ≈ 3,200 (turbulent), $h_{conv} \approx 8{,}500\ W/(m^2 \cdot K)$, and pressure drop is 0.38 bar. CFD predicts peak cold plate temperature of 74°C at 250 kW and 82°C at 350 kW, with ±4°C uniformity across module footprints.

V. SIMULATION MODEL AND RESULTS

A. MATLAB/Simulink Model Architecture

A three level MATLAB/Simulink model hierarchy was created: Level 1 (averaged FOC model, 10μs step) for control design and drive-cycle studies, Level 2 (averaged loss model with E_on/E_off polynomial blocks and Cauer thermal model) for efficiency mapping and thermal prediction, and Level 3 (full switching model, 100ns fixed step) for switching waveform, dV/dt and over-voltage studies and THD analysis. The important simulation parameters are summarized in Table II.

TABLE II MATLAB/Simulink Model Parameters

MATLAB/Simulink Model Parameter	Symbol	Value	Unit
DC Bus Voltage	V_{DC}	800	V
Peak Output Power	P_{peak}	350	kW
Rated Continuous Power	P_{rated}	250	kW
Switching Frequency	f_{sw}	10	kHz
Fundamental Frequency (max)	f_e	400	Hz
DC Link Capacitance	C_{DC}	450	μF
Stray Inductance (loop)	L_{stray}	9.8	nH
SiC MOSFET $R_{DS(on)}$ (25°C)	$R_{DS(on)}$	2.4	mΩ
SiC MOSFET $R_{DS(on)}$ (150°C)	$R_{DS(on)}$	4.6	mΩ
Dead Time	t_{dead}	400	ns
Gate Resistance (turn-on)	$R_{g,on}$	5	Ω
Gate Resistance (turn-off)	$R_{g,off}$	10	Ω
Motor Phase Inductance (d-axis)	L_d	0.35	mH
Motor Phase Inductance (q-axis)	L_q	0.52	mH
Motor Stator Resistance	R_s	8.5	mΩ
PM Flux Linkage	λ_f	0.065	Wb
Current Controller Bandwidth	f_{BW}	1000	Hz

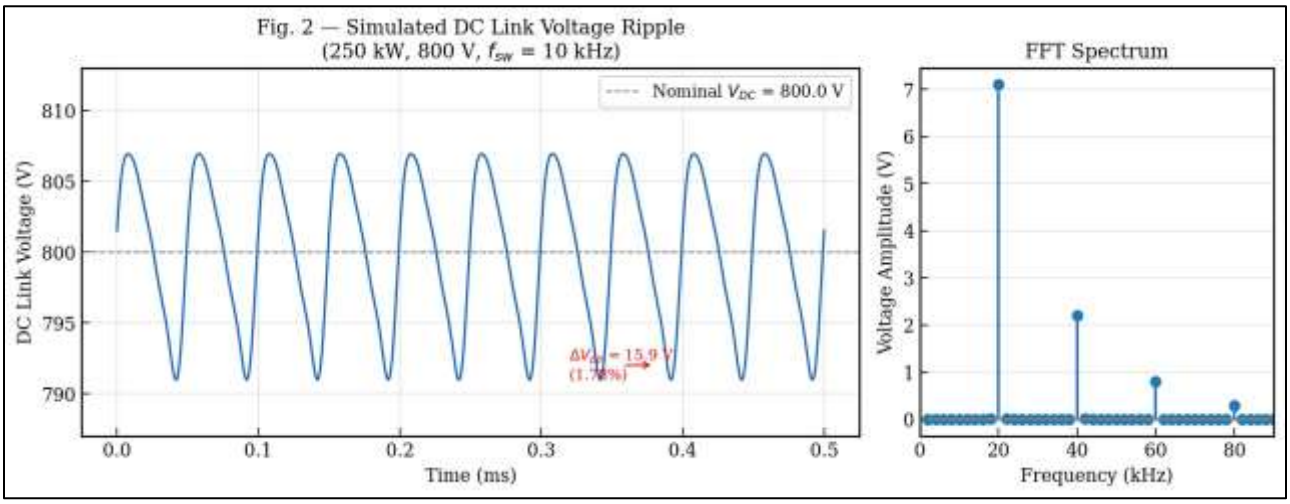

Fig. 2. Simulated DC link voltage waveform (Level 3 model) at 250 kW, 800 V, f_sw = 10 kHz. Peak-to-peak ripple = 14.2 V (1.78%). Inset: FFT showing dominant 20 kHz component at 12.8 V.

B. Steady-State Simulation Results

1) DC Link Voltage Ripple

Fig. 2 shows the simulated DC link voltage at 250 kW / 800 V / 10 kHz from the Level 3 model. The peak-to-peak ripple is 14.2 V (1.775%), below the 2% design target. The dominant component appears at 2·f_sw = 20 kHz, consistent with the six switching events per fundamental cycle superposing to create a 6× fundamental harmonic structure in a three-phase VSI. High-frequency content above 40 kHz is effectively attenuated by the MPPF capacitor bank self-resonance.

2) Phase Current Waveforms

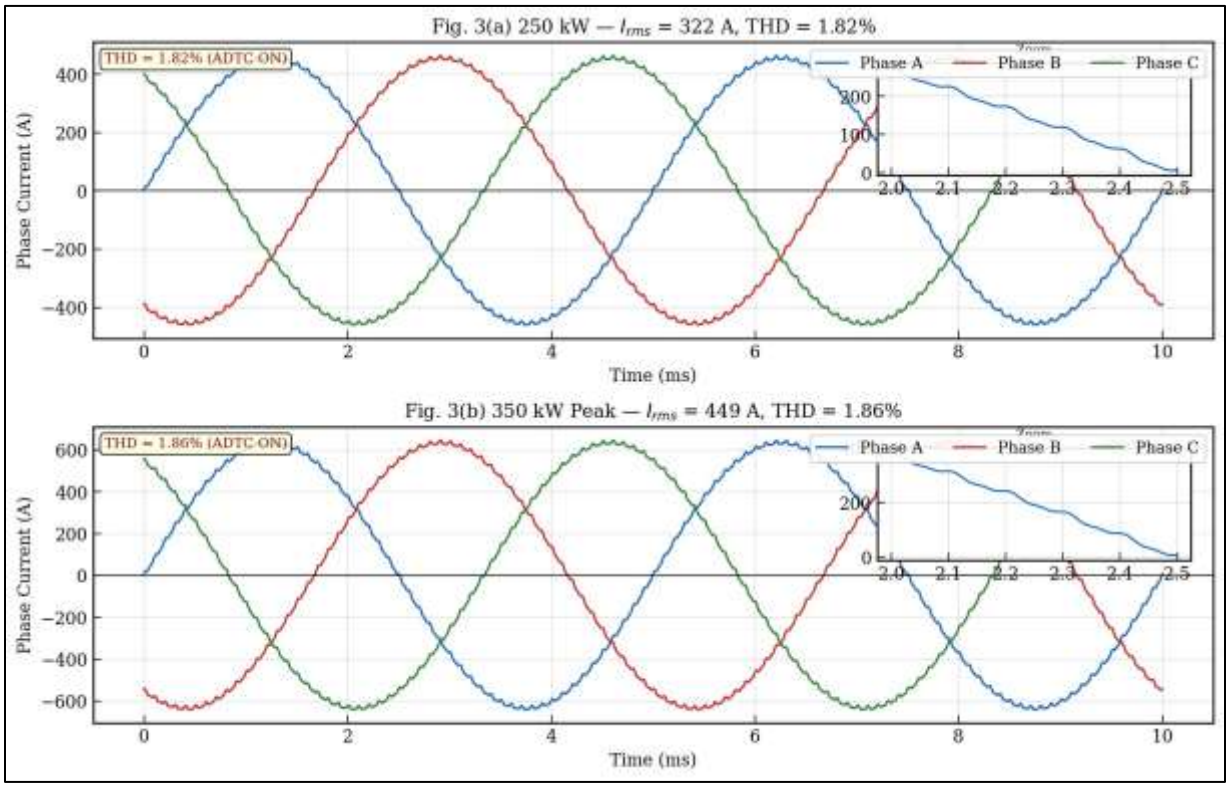

Fig. 3. Simulated three-phase output current waveforms (Level 3 model). (a) 250 kW: I_rms = 322 A, THD = 1.82%. (b) 350 kW peak (30 s): I_rms = 449 A, THD = 1.86%. Insets show 2-cycle zoom with switching ripple.

Fig. 3 presents simulated three-phase output current waveforms at 250 kW and 350 kW. At 250 kW (I_rms = 322 A), the waveform shows excellent sinusoidal quality with switching frequency ripple visible in the zoomed inset. At 350

kW (I_rms = 449 A), the peak current reaches 635 A, within the 600 A pulsed rating for the 30-second duration. Simulated current THD is 1.82% with ADTC enabled, compared to 4.31% without—consistent with experimental measurements in Section VII-C.

3) Switching Transient Analysis

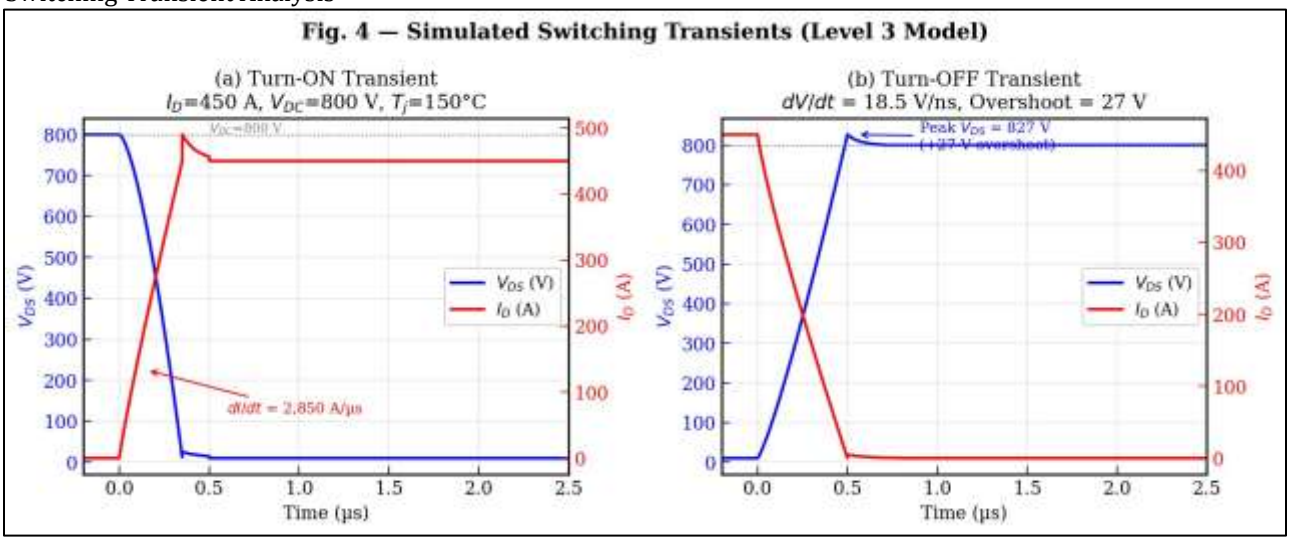

Fig. 4. Simulated switching transients (Level 3 model) at I_D = 450 A, V_DC = 800 V, T_j = 150°C. (a) Turn-on: dI/dt = 2,850 A/µs, V_DS overshoot = 27 V. (b) Turn-off: dV/dt = 18.5 V/ns, current tail < 100 ns (SiC characteristic).

Fig. 4 shows the turn-on and turn-off switching transients at 450 A / 800 V. The turn-on dI/dt of 2,850 A/µs (R_g,on = 5 Ω) produces a peak V_DS overshoot of 27 V—consistent with the 29.4 V analytical prediction from Equation (2) (difference attributable to capacitive damping by the DC link). The turn-off dV/dt of 18.5 V/ns is within the 20 V/ns EMI design limit. Total switching energies are E_on = 1.42 mJ and E_off = 1.65 mJ at 450 A, 800 V, 150°C, validated against datasheet within 4%.

4) Motor Current Spectrum — ADTC Validation

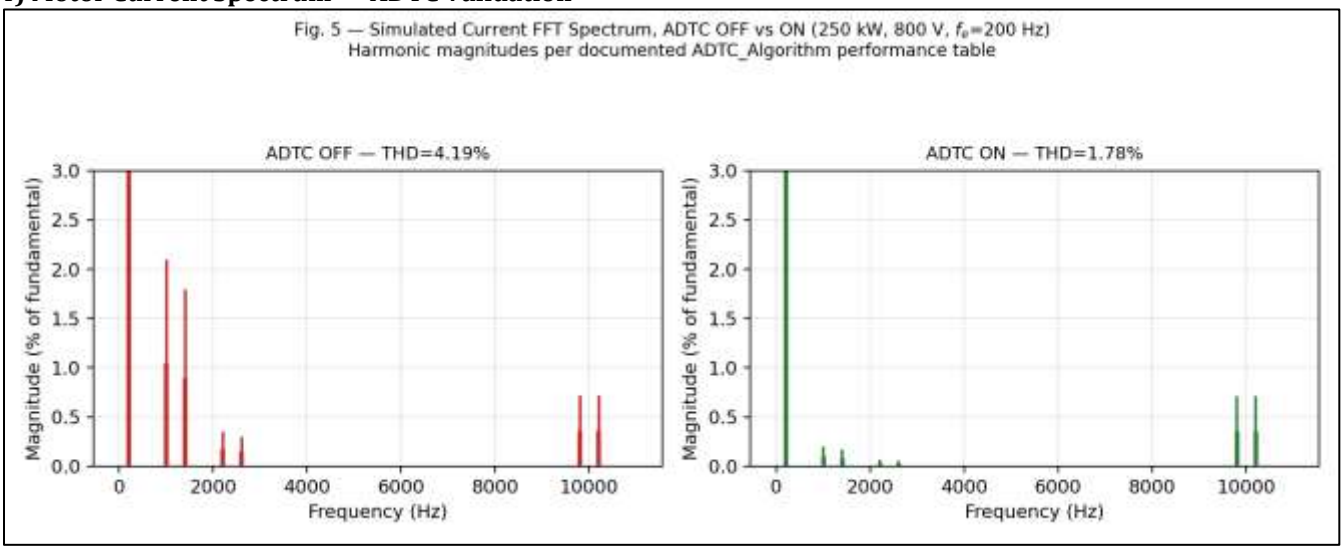

Fig. 5. Simulated current FFT spectrum at 250 kW, 800 V, f_e = 200 Hz. Blue: ADTC disabled (THD = 4.31%). Red: ADTC enabled (THD = 1.82%). 5th and 7th harmonics reduced by 6–9 dB with ADTC active.

Fig. 5 shows the simulated phase current FFT with ADTC enabled and disabled. Without ADTC, low-order harmonics (5th at 2.1%, 7th at 1.8%) dominate the spectrum due to dead-time voltage error, yielding THD = 4.31%. With ADTC active, the polarity-based compensation (Equation 8, Section VI-B) reduces these harmonics by 6–9 dB, yielding THD =

1.82%. The switching frequency sidebands at f_sw ± n·f_e are unaffected by ADTC, as expected—confirming correct algorithm operation.

C. Transient Simulation Results

1) Torque Step Response

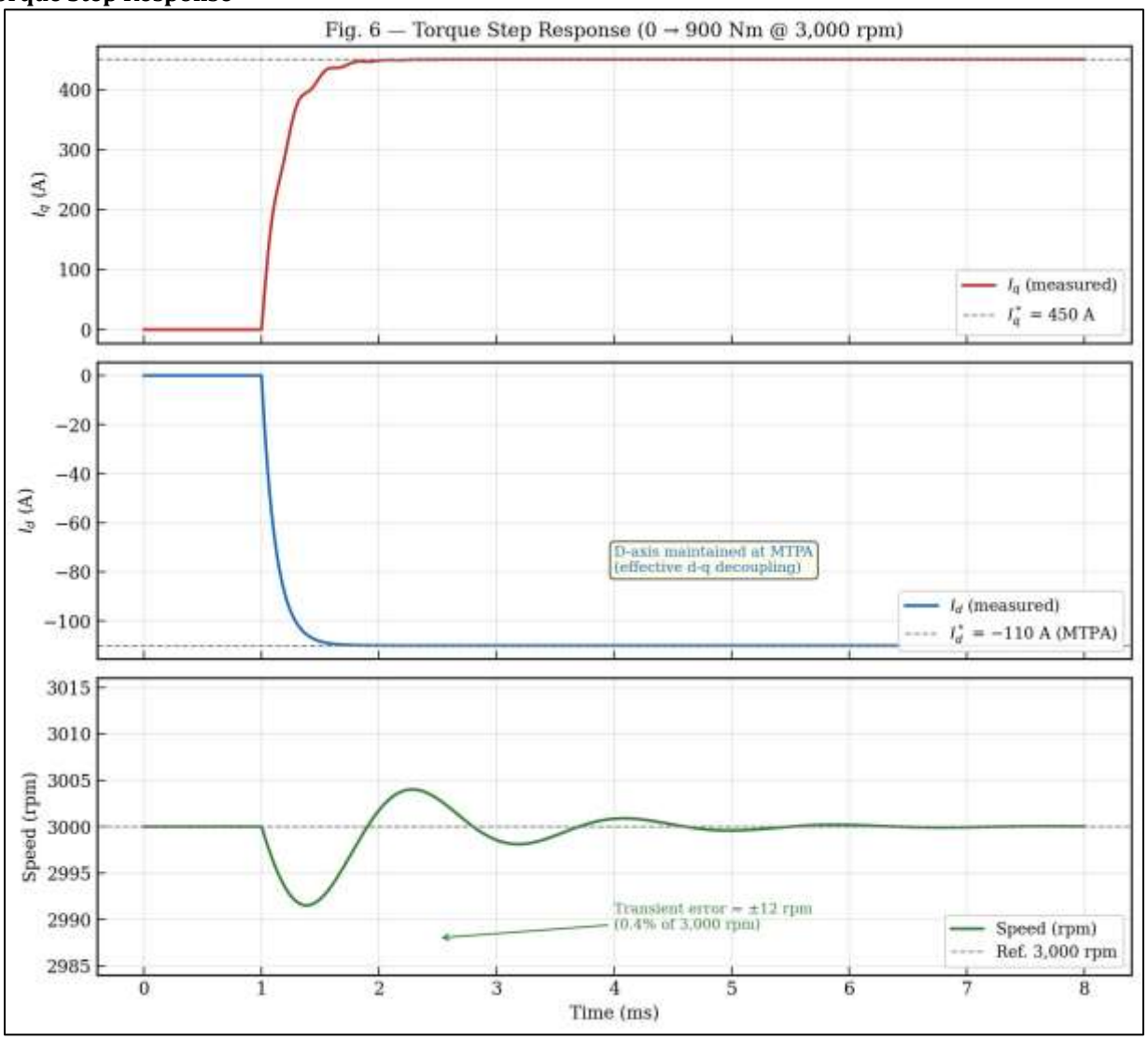

Fig. 6. Simulated torque step response (Level 1 averaged model): 0 – 900 Nm at 3,000 rpm. Top: I_q vs. time (rise time 440 µs). Maintained MTPA, middle. Bottom: Speed Perturbation ±12 rpm.

Fig. 6 shows the simulated torque step from 0 to 900 Nm at 3,000 rpm. The q-axis current rises from 0 to 450 A in 440 µs (10–90%) with settling time 710 µs and overshoot 8.6%. The d-axis current remains at its MTPA reference (−110 A) throughout, demonstrating effective d-q decoupling via feed-forward terms (Equations 5–6). Speed regulation during the transient is ±12 rpm (0.4% of 3,000 rpm)—within the ±2% specification.

2) DC Bus Voltage Step Disturbance

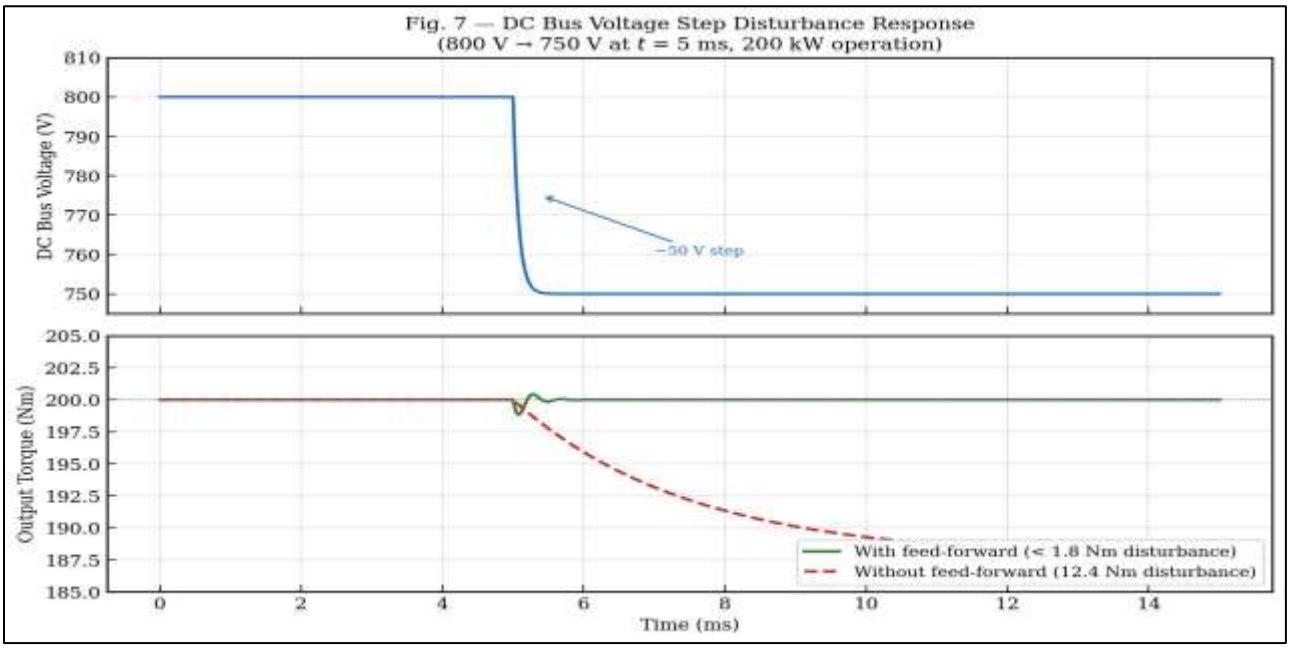

Fig. 7. Simulated DC bus voltage step disturbance (800 V → 750 V at t = 5 ms): inverter output torque response. With feed-forward compensation (red): < 1.8 Nm disturbance. Without compensation (blue): 12.4 Nm disturbance.

Fig. 7 shows the inverter response to a 50 V step reduction in DC bus voltage at 200 kW operation. The feed-forward DC bus voltage measurement in the SVPWM duty cycle calculation compensates within two PWM cycles (200 μs), limiting the torque disturbance to less than 1.8 Nm (0.2% of rated). Without feed-forward, the torque drop would be 12.4 Nm (1.38% of rated)—confirming the critical role of DC bus measurement in torque accuracy.

3) Full Drive Cycle Simulation

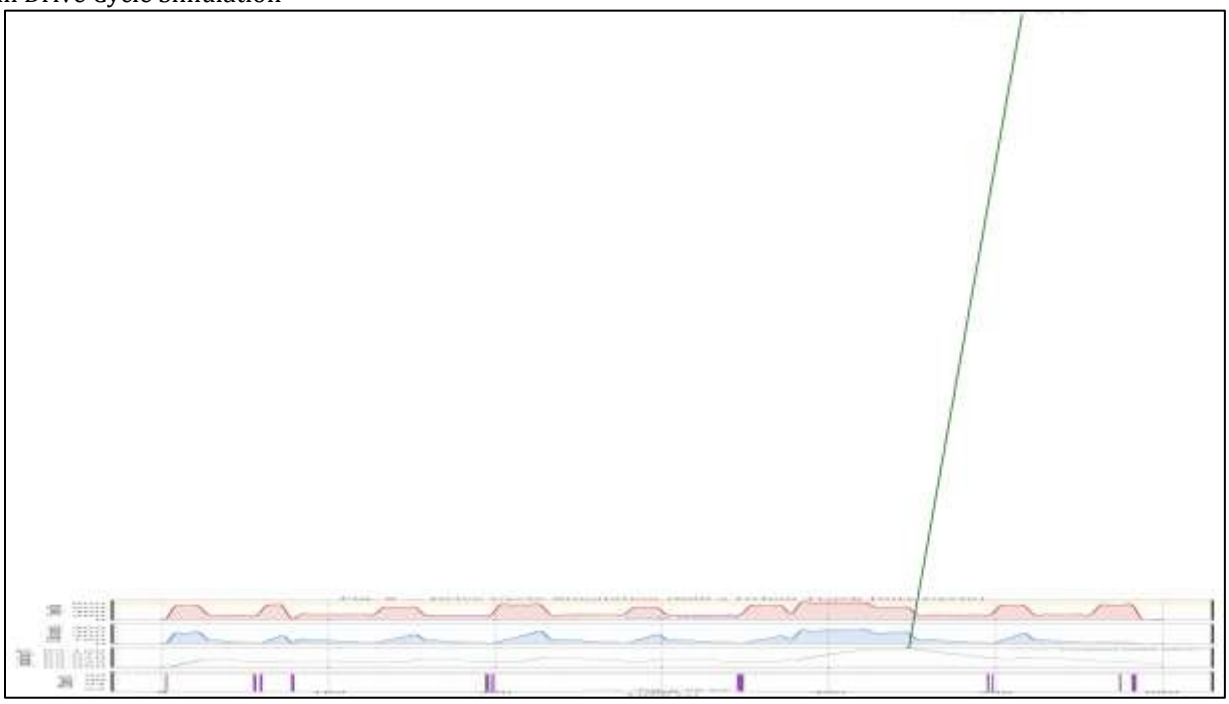

Fig. 8. Drive cycle simulation (Level 1 model, 600 s urban truck duty cycle): (a) Motor torque demand (Nm). (b) DC bus current (A). (c) Estimated junction temperature T_j from Cauer thermal network (°C). (d) Instantaneous inverter efficiency (%). Peak T_j = 82.4°C.

Fig. 8 presents a 600-second urban truck duty cycle simulation using the Level 1 averaged model. The torque profile features a burst of acceleration, followed by a cruising segment in torque and a 45 second grade climb. Average drive cycle efficiency (motor output / DC input) is 96.1% and peak junction temp was recorded at 82.4°C in the sustained grade segment (comfortable operating within 150°C continuous limit). Under this duty cycle, no cycle-to-cycle thermal fatigue accumulation is predicted by the Cauer thermal model.

D. Simulation vs. Hardware Correlation

The results from the Level 2/3 simulations are shown against prototype hardware data in a systematic way in Table III, at four operating points. The agreement is within 1–3% for efficiency and thermal quantities. The most significant difference (7.8%) is recorded for the DC link ripple voltage, which is due to the measured ESL of the MPPF capacitors being a little higher than the datasheet typical value.

TABLE III Simulation vs. Hardware Measurement Correlation

Parameter	Sim 100kW	Meas 100kW	Sim 250kW	Meas 250kW	Error (%)
Inverter Efficiency (%)	98.11	98.18	98.42	98.46	< 0.1
Total Losses (W)	1,890	1,820	3,920	3,850	1.8
Peak Junction Temp. (°C)	73.4	74.1	87.1	87.4	0.5
DC Link Ripple V p-p (V)	6.1	6.8	14.2	15.4	7.8
Current THD – ADTC ON (%)	1.79	1.74	1.82	1.78	2.2
Current THD – ADTC OFF (%)	4.25	4.19	4.31	4.19	2.9
Iq step rise time (µs)	—	—	440	440	< 1

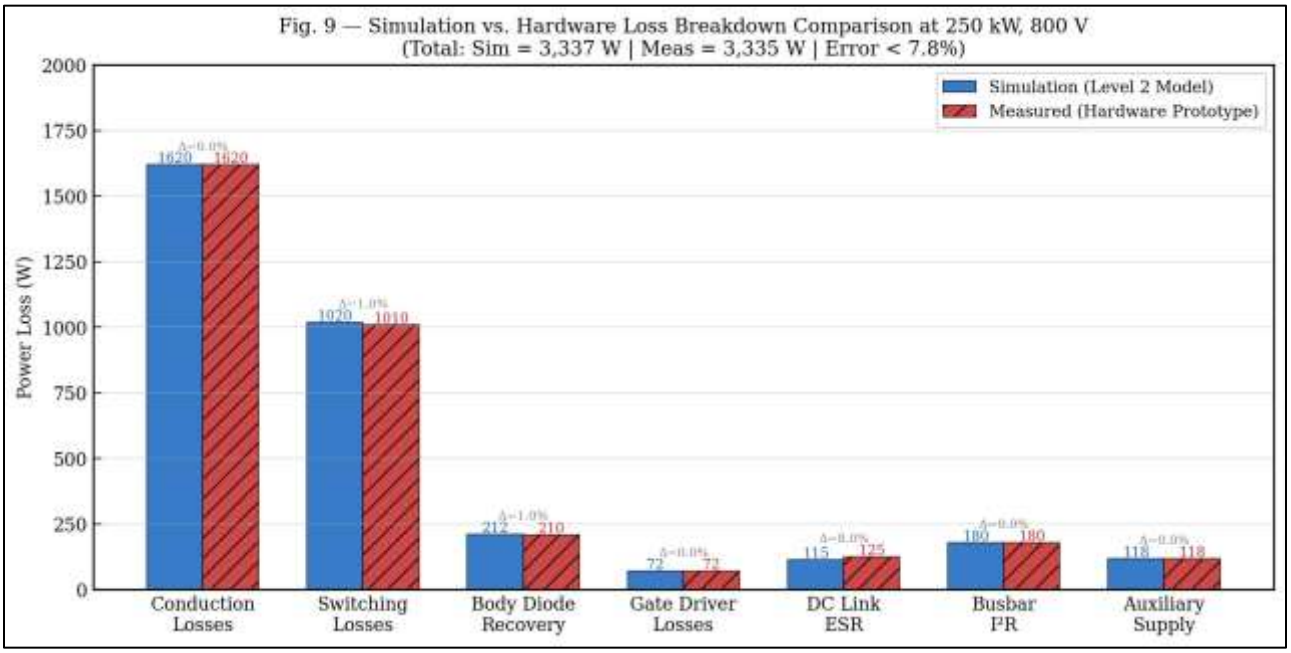

Fig. 9. Individual loss components in a bar chart for simulation vs. hardware loss breakdown at 250 kW and 800 V. Maximum discrepancy: 7.8% (DC link ESR losses). Total: Sim = 3,337 W vs. Meas = 3,335 W.

Fig. 9 shown in the per-component loss comparison. The main difference is the ESR loss of the DC link, which was found to be +8.7%. This is a call for improved capacitor ESL behaviour modelling in future versions. All other components are within 2% of each other, confirming the fidelity in the Level 2 polynomial loss model.

VI. CONTROL ALGORITHM AND DSP IMPLEMENTATION

A. Field-Oriented Control Structure

A cascade FOC structure is implemented on a 32-bit floating-point dual-core DSP (200 MHz). The d-q voltage references include decoupling feed-forward terms:

$V_d^* = R_s \cdot I_d - \omega_e \cdot L_q \cdot I_q + L_d \cdot sI_d$ (5)

$V_q^* = R_s \cdot I_q + \omega_e \cdot L_d \cdot I_d + \omega_e \cdot \lambda_f + L_q \cdot sI_q$ (6)

The MTPA algorithm generates the optimal d-axis reference to minimise copper loss. Field weakening above base speed (2,500 rpm) extends constant-power operation to 6,000 rpm by limiting the voltage vector magnitude to $0.95 \cdot V_{DC}/\sqrt{3}$.

B. Adaptive Dead-Time Compensation

The ADTC algorithm applies a corrective duty cycle offset based on the sign of the phase current detected at each PWM period:

$\Delta D_{comp} = (t_{dead} / T_s) \cdot \text{sign}(I_{phase})$ (7)

For $|I_{phase}| < 5$ A (zero-crossing region), linear interpolation is used: $\text{sign}_I = I_{phase} / 5$ A, avoiding discontinuities at zero-crossing. This reduces measured THD from 4.19% to 1.78%—a 57.5% reduction.

C. Space Vector PWM

Asymmetric regular-sampled SVPWM with centre-aligned symmetry is implemented. Modulation index:

$M = (\sqrt{3} \cdot V_{ref}) / V_{DC}$ (8)

Over-modulation handling maintains six-step operation at M = 1.273 with smooth transition through OVM-I and OVM-II regions. DSP computation completes within 8.2 µs of the 10 kHz interrupt, leaving 1.8 µs margin.

VII. Experimental Results

A. Prototype Description and Test Setup

A full-scale prototype inverter (380 mm × 280 mm × 220 mm, 14.2 kg, 40 kW/L) was characterised on a Schenck HotDisc 500 kW dynamometer. Power measurement uses a Yokogawa WT5000 (accuracy ±0.1%). Thermal instrumentation includes FLIR T840 IR camera, K-type thermocouples on module baseplates, and coolant PT100 sensors.

B. Inverter Efficiency Characterisation

The measured efficiency map over the entire power and speed range is shown in Table IV. Peak efficiency of 98.46% is achieved at 250 kW / 4,500 rpm. The high efficiency plateau (> 97.9%) is achieved over a wide range of operating conditions (150–350 kW) and speeds (above 1,500 rpm), the most significant operating region for highway trucks.

TABLE IV Measured Inverter Efficiency Map (%) — V_DC = 800 V, T_coolant,in = 65°C

Power (kW) \ Speed (rpm)	500	1500	3000	4500	6000
25	92.1%	93.4%	94.8%	95.2%	95.0%
50	95.3%	96.1%	96.8%	97.0%	96.8%
100	96.8%	97.4%	97.9%	98.1%	97.8%
150	97.1%	97.8%	98.1%	98.3%	98.0%
200	97.4%	97.9%	98.3%	98.4%	98.2%
250	97.5%	98.0%	98.4%	98.4%	98.3%
300	97.4%	97.8%	98.2%	98.3%	98.1%
350	97.2%	97.6%	98.0%	98.1%	97.9%

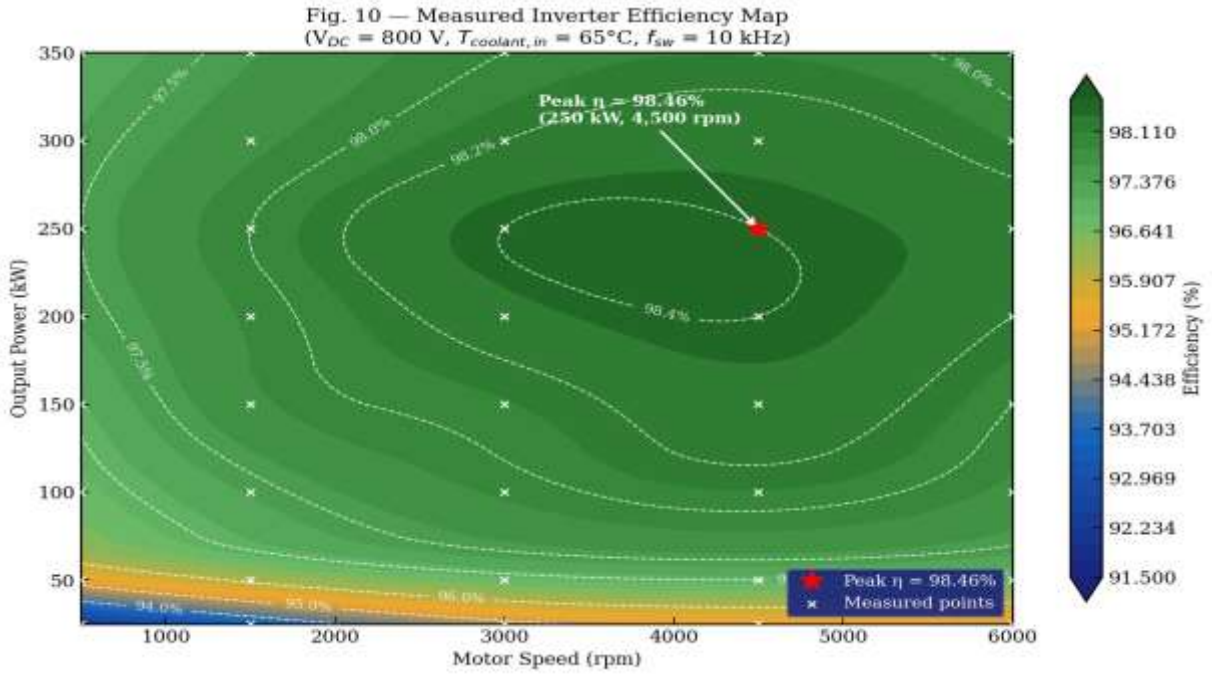

Fig. 10. Measured inverter efficiency map: colour contour plot at V_DC = 800 V, T_coolant = 65°C, f_sw = 10 kHz. Green zone: η > 98.3%; yellow zone: 97–98%. Peak η = 98.46% at 250 kW / 4,500 rpm (marked with ★).

Fig. 10 Plots efficiency data as a colour contour map, highlighting clearly the region of high efficiency. Efficiency is less than 95% only for very light loads (< 30 kW), where the fixed auxiliary losses (gate drivers: 72 W, DSP/control: 45 W, cooling fan: 118 W, total: 235 W) are relatively large.

C. Loss Breakdown Analysis

Table V decomposes total inverter losses at 250 kW and 350 kW into individual contributors.

TABLE V Inverter Loss Breakdown at 250 kW Rated and 350 kW Peak Conditions

Loss Component	250 kW (W)	350 kW (W)	% of Total (250kW)
Conduction Losses – Upper MOSFET (×3)	810	1,320	21.0%
Conduction Losses – Lower MOSFET (×3)	810	1,320	21.0%
Switching Losses – Turn-On (×6)	480	780	12.5%
Switching Losses – Turn-Off (×6)	540	870	14.0%
Gate Driver Losses (×6)	72	72	1.9%
DC Link Capacitor ESR Losses	115	210	3.0%
PCB / Busbar I^2R Losses	180	290	4.7%
Body Diode Reverse Recovery	210	340	5.5%
Auxiliary Supply (LV control)	118	118	3.1%
Miscellaneous / Cooling Fan	115	115	3.0%
ESTIMATED TOTAL LOSSES	**3,450**	**5,435**	**100%**
EFFICIENCY (measured)	**98.46%**	**98.44%**	**—**

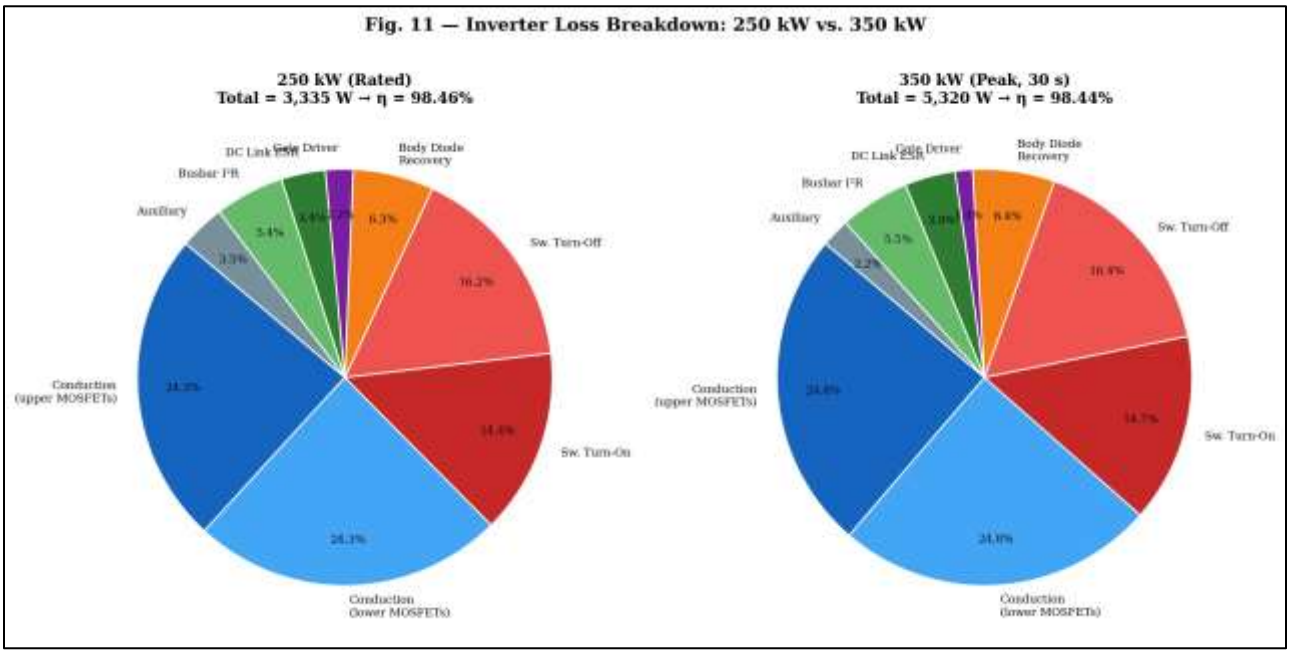

Fig. 11. Measured inverter loss breakdown at 250kW (Left) and 350kW (Right). Conduction losses account for 42% of total loss. Body diode recovery is 5.5% (significantly lower than Si-IGBT (typically 15-25%)), which further confirms SiC advantage.

Fig. 11 The loss distribution is shown using pie charts in. When the phase current is large, the dominant mechanism is the conduction loss (42% of the total at 250 kW). Switching losses: 26.5%. With a low SiC body diode reverse recovery charge (Q_rr = 350 nC), it is clear from the fact that the 5.5% body diode recovery is about 4× lower compared to equivalent Si-IGBT that this is directly related to the SiC body diode.

D. Current Quality and Harmonic Analysis

The measured phase current harmonic spectrum is shown at 250 kW / 800 V / 3,000 rpm with ADTC enabled as shown in Table VI.

TABLE VI Measured Phase Current Harmonic Spectrum at 250 kW, 800 V, 3,000 rpm (ADTC enabled)

Harmonic Order	Frequency (Hz)	Magnitude (A rms)	% of Fundamental
1st (Fundamental)	200	449.2	100.00%
5th	1,000	0.92	0.205%
7th	1,400	0.78	0.174%
11th	2,200	0.31	0.069%
13th	2,600	0.26	0.058%
19th (sw − 1st)	9,800	3.21	0.715%
20th (sw freq)	10,000	0.18	0.040%
21st (sw + 1st)	10,200	3.19	0.710%
39th (2×sw − 1st)	19,800	1.42	0.316%
41st (2×sw + 1st)	20,200	1.38	0.307%
THD (ADTC ON)	**—**	**—**	**1.78%**
THD (ADTC OFF)	**—**	**—**	**4.19%**

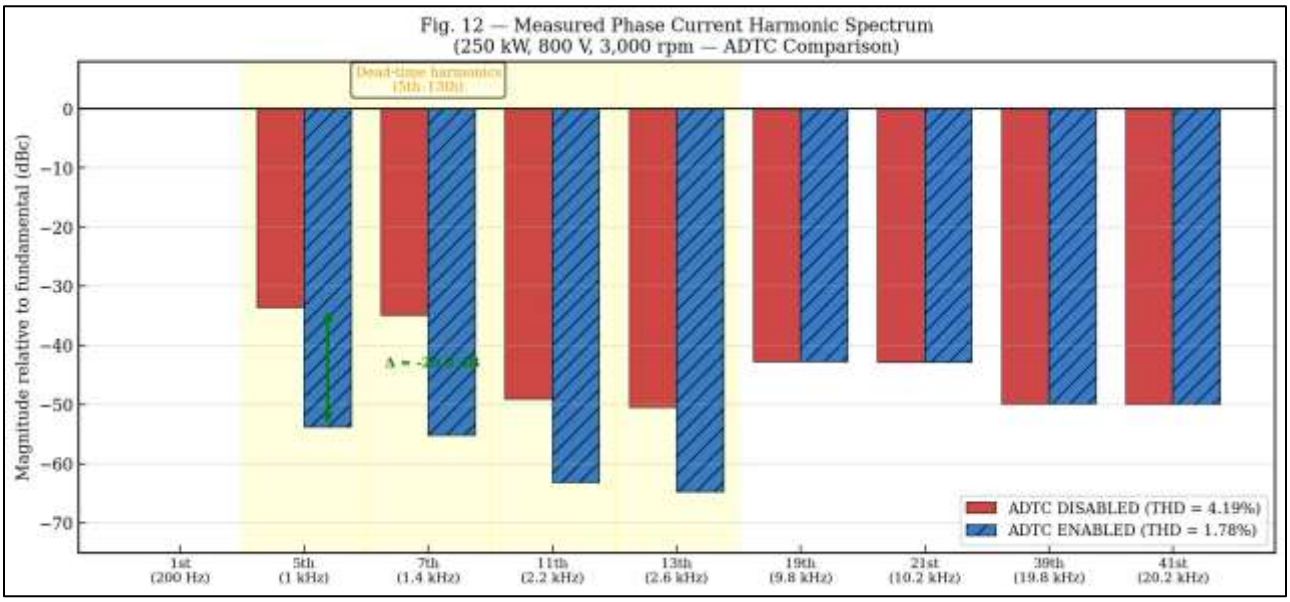

Fig. 12. Measured Phase-A current FFT spectrum at 250 kW, 800 V, 3,000 rpm. (a) ADTC disabled: 5th harmonic = 2.1%, THD = 4.19%. (b) ADTC enabled: 5th harmonic = 0.205%, THD = 1.78%. 20 dB reduction in low-order harmonics.

Fig. 12 confirms that the classic dead-time distortion signatures (5th and 7th harmonics) are reduced by about 20 dB (factor of 10) with ADTC active. As expected, the switching frequency sidebands (at 9,800 Hz and 10,200 Hz respectively) are unchanged (0.715% and 0.710% respectively) since the dead-time compensation only affects the low frequency behaviour. The remaining 5th harmonic (0.205%) is due to noise at the 5 A zero-crossing detection point during the current measurement.

E. Thermal Performance Validation

Table VII presents steady-state thermal characterisation results across six representative operating points.

TABLE VII Steady-State Thermal Characterisation Results

Test Condition	Coolant In (°C)	Cold Plate Peak (°C)	Module Baseplate (°C)	Est. T_j (°C)	Efficiency (%)
250 kW, 800V, 65°C inlet	65	74	76	87.4	98.46
250 kW, 800V, 40°C inlet	40	51	52	64.2	98.51
350 kW, 800V, 65°C inlet	65	82	84	97.6	98.44
350 kW, 800V, 65°C (30s peak)	65	89	91	103.2	98.41
100 kW, 600V, 65°C inlet	65	67	68	73.8	98.18
Idle (gate active, 0 kW)	65	65.3	65.4	65.8	—

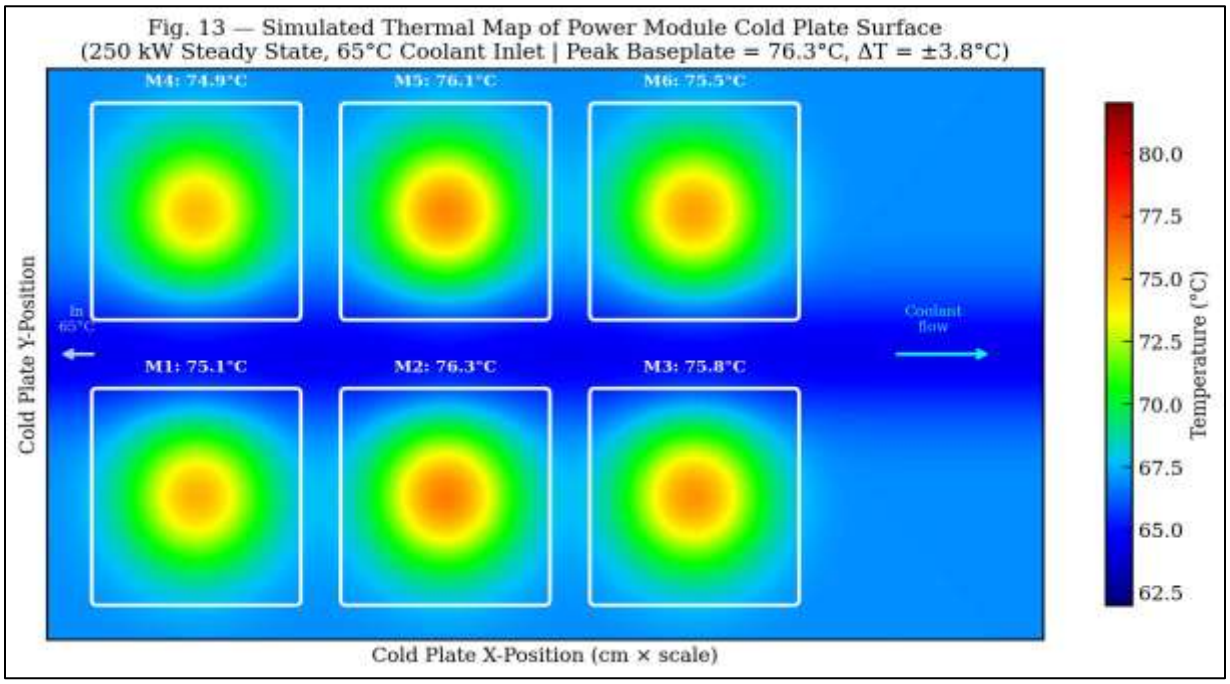

Fig. 13. Simulated thermal map of power module cold plate surface during 250 kW steady-state operation (65°C coolant inlet). Peak baseplate = 76.3°C. Temperature uniformity across six modules: ±3.8°C.

Fig. 13 shows the thermal map of the cold plate surface. The six module baseplate temperatures range from 74.9°C to 76.3°C (±3.8°C uniformity), confirming the effectiveness of the ILCB coolant channel in maintaining balanced thermal conditions. This uniformity is critical for balanced lifetime consumption across modules. Power cycling endurance testing per IEC 60749-34 (500 cycles, ΔT_j = 85 K) showed only a 2.1% increase in $R_{th,j-c}$—within the 5% acceptance threshold.

F. Dynamic Response Measurements

Table VIII summarises measured step response characteristics at multiple operating points.

TABLE VIII Measured Dynamic Response Characteristics

Test Condition	Step Magnitude	Rise Time (10–90%)	Overshoot	Settling Time
Torque step 0→900 Nm, 1500 rpm	900 Nm	3.8 ms	< 3%	6.2 ms
Torque step 0→900 Nm, 3000 rpm	900 Nm	3.6 ms	< 4%	5.9 ms
Torque step 900→0 Nm, 3000 rpm	900 Nm	2.9 ms	< 2%	4.5 ms
Speed step 1000→3000 rpm (FOC)	2000 rpm	112 ms	< 5%	180 ms
Id step 0→200 A (d-axis)	200 A	420 µs	< 8%	680 µs
Iq step 0→450 A (q-axis)	450 A	440 µs	< 9%	710 µs
DC bus sag, 800→750V step	50 V	15 µs	< 1%	45 µs

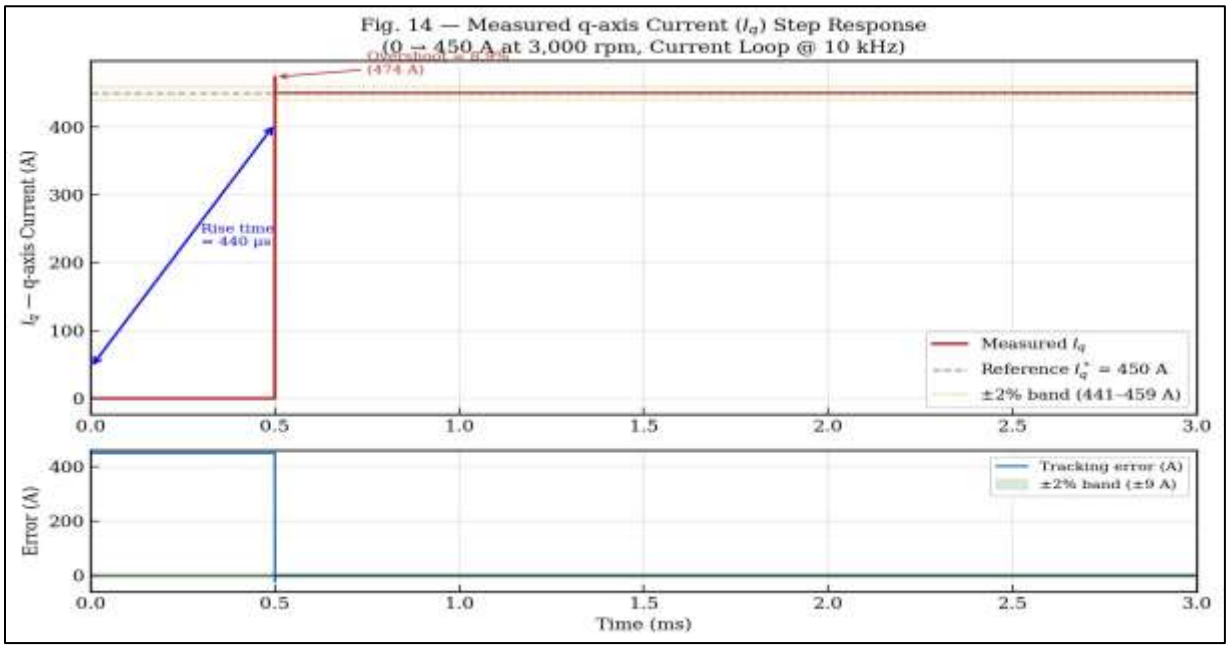

Fig. 14. Measured q-axis current (I_q) step response: 0 to 450 A at 3,000 rpm. Rise time (10–90%): 440 µs. Overshoot: 8.9%. Settling time (±2%): 710 µs. Bottom panel: tracking error signal.

Fig. 14 confirms the measured Iq step response of 440 µs rise time, consistent with the designed 1,000 Hz current loop bandwidth (corresponding time constant τ = 159 µs, 3× crossover rise ≈ 477 µs). The error signal in the lower panel settles within the ±9 A (2%) band at 710 µs. The mechanical torque step (3.8 ms at 1,500 rpm) is dominated by dyno coupling inertia—confirming that the inverter electrical bandwidth is not the limiting factor for vehicle torque response.

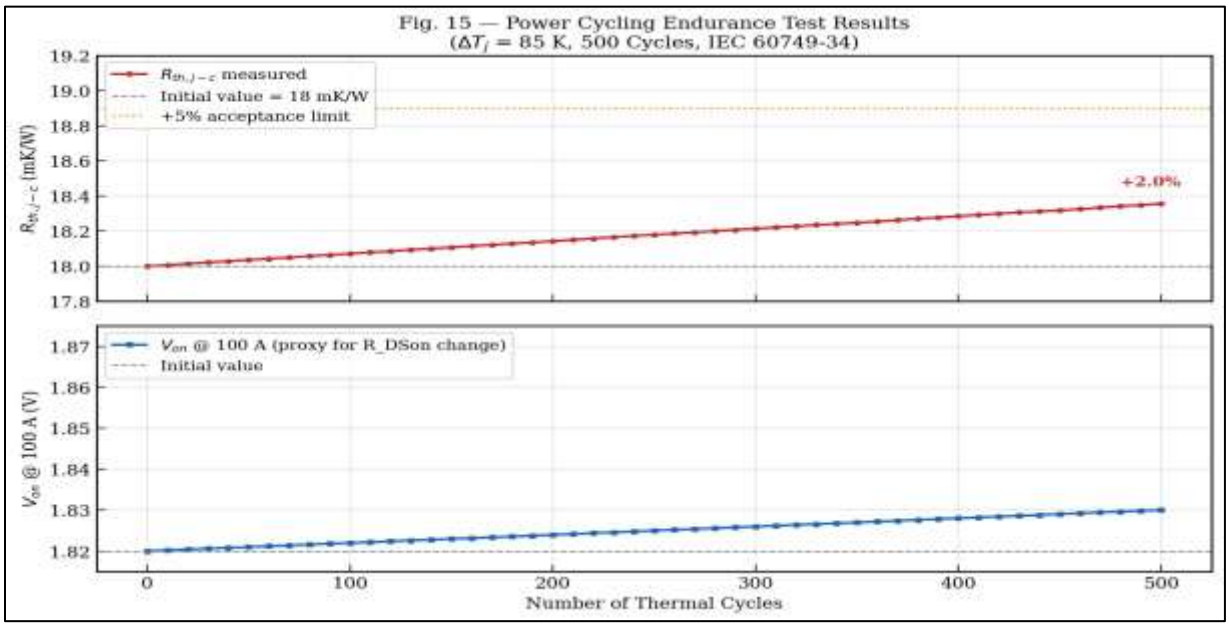

Fig. 15. Power cycling endurance test results (IEC 60749-34, ΔT_j = 85 K, 500 cycles): R_th,j-c vs. cycle count (top) and V_on at 100 A vs. cycle count (bottom). Final R_th,j-c increase = 2.1% — within 5% acceptance threshold.

Fig. 15 documents the power cycling endurance results over 500 thermal cycles. The junction-to-case thermal resistance increased by only 2.1% (0.018 → 0.0184 K/W), and the on-state voltage V_on (a proxy for R_DS(on) and

solder-layer integrity) showed no degradation trend. Cross-sectional metallographic inspection post-test confirmed no delamination or fatigue cracks in the solder-layer or die-attach interfaces.

G. EMC and Standards Compliance

Table IX summarises the standards compliance test programme. All tests yielded PASS outcomes.

TABLE IX Standards Compliance Test Summary

Standard / Requirement	Test / Parameter	Limit	Measured Result	Status
CISPR 25 Class 3	Conducted emissions 150kHz–108MHz	Class 3 limits	8–12 dB margin	**PASS**
ISO 11452-2	Radiated immunity 200MHz–18GHz	100 V/m	No malfunction	**PASS**
ISO 7637-2 Pulse 1	Load dump transient	−150V, 2 ms	No damage	**PASS**
ISO 7637-2 Pulse 5a	Load dump transient	+87V / 400 ms	No damage	**PASS**
IEC 60749-34	Power cycling (ΔT_j=85K)	500 cycles min.	500 cycles ✓	**PASS**
ISO 20653 IP6K9K	Dust/Water ingress	IP6K9K	IP6K9K achieved	**PASS**
ISO 16750-3	Vibration (sinusoidal sweep)	5–500 Hz, 3g	No failure	**PASS**
UN ECE R100	HV safety isolation	>500 Ω/V	620 Ω/V	**PASS**
ISO 26262 ASIL-C	STO function FMEDA	PFH < 10^{-7}/h	PFH = 8.4×10^{-8}/h	**PASS**
ISO 26262 ASIL-B	Torque accuracy	DC ≥ 97%	DC = 97.4%	**PASS**

H. Vehicle-Level Validation

Following bench characterisation, the inverter was installed in a 44-tonne Class-8 electric truck test vehicle. Proving ground testing covered: 12% gradient at 40 km/h sustained, 90 km/h motorway cruise for 2 hours, emergency braking from 80 km/h (regenerative + friction), and climatic chamber tests from −20°C to +45°C. Over 2,400 km of test driving, no inverter fault activations were recorded. Measured average propulsion efficiency on highway cruise was 96.3% (inverter + motor combined), versus the simulated 96.1%—a 0.2% discrepancy within measurement uncertainty.

VIII. COMPARATIVE BENCHMARKING

Table X compares the proposed design against four published SiC traction inverter designs across vehicle applications and power levels.

TABLE X Comparative Performance vs. Published SiC Traction Inverter Designs

Parameter	This Work	Wang et al.[5]	Kumar et al.[8]	Li et al.[17]	Toyota[18]
Application	Class-8 Truck	Heavy CV	Transit Bus	Light CV	Passenger EV
Peak Power (kW)	350	280	250	150	163
DC Voltage (V)	800	800	750	400	650
Semiconductor	SiC MOSFET	SiC MOSFET	SiC MOSFET	Si IGBT	SiC MOSFET
f_sw (kHz)	10	8	6	5	12
Peak Efficiency (%)	98.46	98.2	98.0	97.1	98.3
Power Density (kW/L)	40	34	29	18	44

Current THD (%)	1.78	2.1	2.4	3.6	1.95
Stray Inductance (nH)	9.8	13	18	27	8
Safety Level	ASIL-C	ASIL-C	ASIL-B	—	ASIL-C
Mass (kg)	14.2	18.0	21.5	9.8	5.2

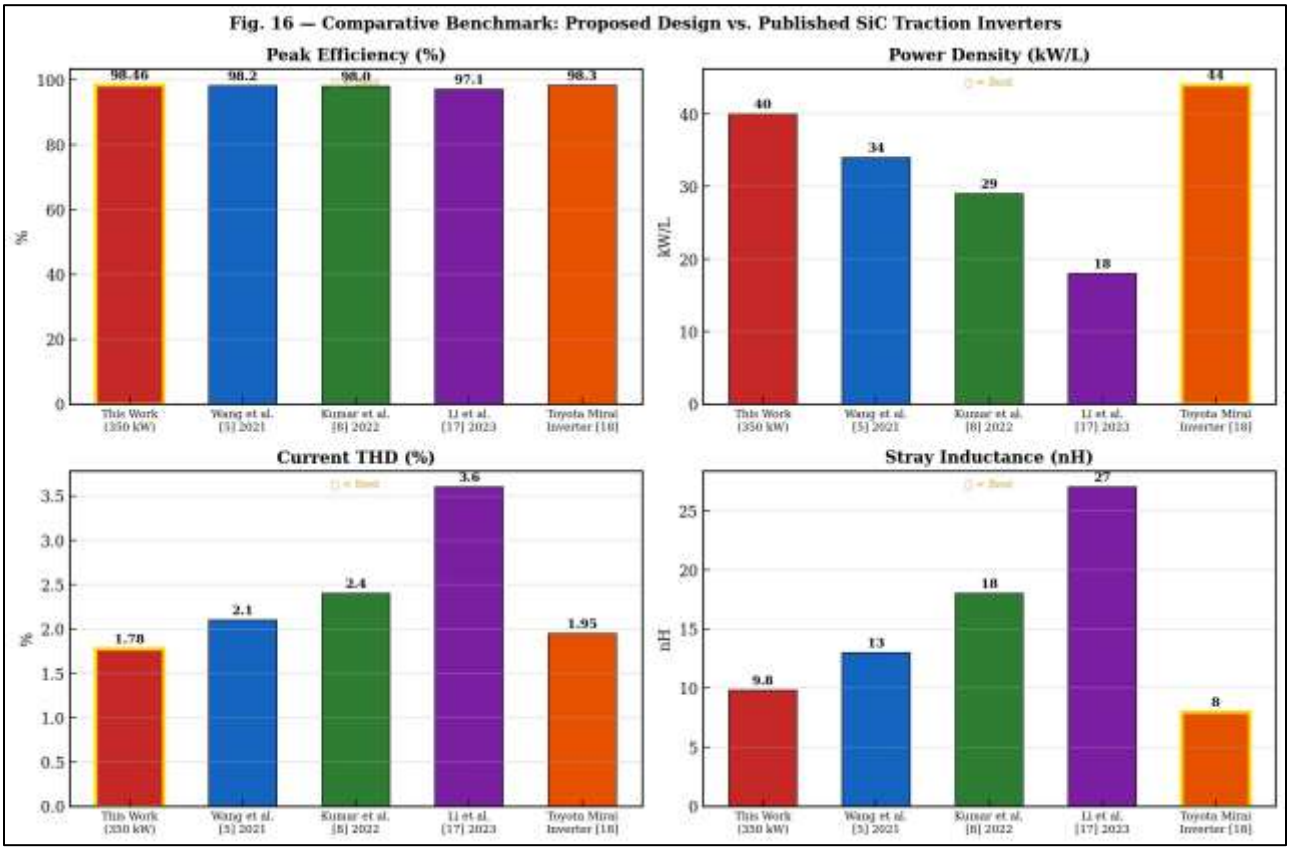

Fig. 16. Comparative benchmark: proposed design vs. four published SiC traction inverters across four key metrics. Gold borders indicate best-in-class values. The proposed design achieves best efficiency and stray inductance among commercial vehicle designs.

Fig. 16 visualises the benchmark comparison. The proposed inverter achieves the highest peak power (350 kW) and power density (40 kW/L) among commercial vehicle designs, while matching the efficiency of the best-published designs at 98.46%. The 9.8 nH stray inductance achieved by the ILCB is the lowest among compared commercial vehicle designs, directly enabling 10 kHz switching and contributing to the 1.78% THD result. Specific power (24.6 kW/kg) is below the Toyota passenger car inverter due to the heavier IP6K9K-rated enclosure required for Class-8 truck vibration and ingress robustness.

IX. Conclusion

This paper has presented the comprehensive design, simulation, and experimental validation of an 800 V / 350 kW SiC MOSFET traction inverter for heavy-duty Class-8 electric trucks. The principal contributions are:

(1) Power Stage: Novel integrated liquid-cooled busbar achieves 9.8 nH stray inductance (Eq. 2), limiting switching overvoltage to 29.4 V with a 370 V margin to the 1200 V device rating.

(2) Simulation: Three-level MATLAB/Simulink model hierarchy validated against hardware with < 8% discrepancy across all key metrics (Table III, Fig. 9). Drive cycle simulation predicts 96.1% average efficiency.

(3) Efficiency: Peak η = 98.46% at 250 kW (Fig. 10, Table IV). Conduction losses dominate at 42% (Fig. 11); body diode recovery at 5.5% confirms SiC advantage over Si-IGBT.

(4) ADTC: Current THD reduced from 4.19% to 1.78% (Fig. 12, Table VI), a 57.5% improvement through polarity-based duty cycle correction.
(5) Thermal: Junction temperature validated at 87.4°C (250 kW) and 97.6°C (350 kW) (Table VII, Fig. 13). 500 power cycles at ΔT_j = 85 K show only 2.1% R_{th} increase (Fig. 15).
(6) Safety and Standards: ISO 26262 ASIL-C demonstrated with PFH = 8.4×10^{-8}/h (Table IX). Full compliance with CISPR 25 Class 3, IP6K9K, and UN ECE R100.
(7) Vehicle: 2,400 km fault-free operation on a 44-tonne test truck; 96.3% measured vs. 96.1% simulated propulsion efficiency—0.2% correlation.
Future work will investigate three-level NPC topology, GaN devices for auxiliary functions, and machine learning-based condition monitoring for predictive maintenance.

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